EXHIBIT G

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PHENIX LONGHORN LLC,

Plaintiff,

v.

AU OPTRONICS CORPORATION, HISENSE ELECTRONICA MEXICO, S.A. DE C.V., HISENSE USA CORPORATION, and DOES 1–10,

Defendants.

CASE NO. 2:23-CV-00477-RWS-RSP

DECLARATION OF ARIS SILZARS REGARDING CLAIM CONSTRUCTION OF U.S. PATENT NOS. 7,233,305 AND 7,557,788

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I. INTRODUCTION

1. I have been retained by Defendants AUO Corporation ("AUO"), Hisense Electronica Mexico, S.A. de C.V., Hisense USA Corporation, and Hisense Visual Technology Co., Ltd. (collectively, "Hisense" and together with AUO, "Defendants") to investigate and opine on certain issues relating to U.S. Patent Nos. 7,233,305 (the "'305 patent") and 7,557,788 (the "'788 patent") (collectively, the "Asserted Patents") asserted by Plaintiff Phenix Longhorn LLC ("Phenix") against Defendants.

2. This declaration is directed to the proper construction of disputed claim terms of the Asserted Patents.

II. QUALIFICATIONS

3. A copy of my curriculum vitae is attached as Appendix 1 to this Declaration. I received a B.A. degree in Physics from Reed College in 1963, an M.S. degree in Physics from the University of Utah in 1965, and a Ph.D. degree in Electrical Engineering from the University of Utah in 1969.

4. I have been an active participant in the development of display technologies and products that use displays since 1974. I have managed research groups as large as 350 technologists in creating and implementing display technologies and high-performance electronic circuits into products based on these technologies. In this experience, I have seen the importance of understanding how a product will be used and how chosen performance features will determine the predominant final product application.

5. I have an intimate knowledge of the state of display–related product developments, and can accurately reflect the current state of these developments. I have participated in numerous technical conference activities (including as Program and General Chair for the International Society for Information Display Symposium – the preeminent annual international conference on

display technology) and made numerous presentations of display applications and on the technology evolution of those products. I was President of the Society for Information Display ("SID") from 2000 – 2002. I am an industry consultant with a broad client base and continue to be active and knowledgeable regarding all new display-related technologies.

6. In my many years of engineering, manufacturing, and product development experience, I have personally been involved in the design of Liquid Crystal Displays (LCDs) and products based on those displays. I have managed new technology based businesses with full responsibility for technology and product strategy, marketing, and financial results. Over the last 25 years I have established my own laboratory for testing display products and analyzing display technology. I am familiar with industry-recognized display standards. With this broad knowledge of display-related products and business operations, I believe that I am qualified to provide an accurate assessment of the technical and business related issues in this case.

III. COMPENSATION

7. I am being compensated at an hourly rate of $375 for my time spent on this case. I receive no other form of compensation related to this case and no part of my compensation depends on the outcome of this case.

IV. SCOPE OF WORK

8. I have been asked to prepare a declaration presenting my opinions on the construction of certain disputed claim terms in the Asserted Patents.

9. My opinions generally relate to the claims that Phenix has accused Defendants of infringing. I refer to this combined group as the "Asserted Claims." The following is a chart of the Asserted Claims.

Asserted Patent	**Asserted Claims**
U.S. Patent No. 7,233,305	1, 2, 5

U.S. Patent No. 7,557,788	1

V. REVIEW AND USE OF DOCUMENTS AND OTHER MATERIALS

10. Materials that I have reviewed and considered are the Asserted Patents, the correspondence prosecution file history for the Asserted Patents, the references cited and considered during prosecution of the Asserted Patents, materials from *Wistron Corporation v. Phenix Longhorn, LLC*, IPR2018-01255 (the "Wistron IPR"), materials from *Innolux Corporation v. Phenix Longhorn LLC*, IPR2025-00044 (the "Innolux '788 IPR"), *Innolux Corporation v. Phenix Longhorn LLC*, IPR2025-00043 (the "Innolux '305 IPR"), materials from *Phenix Longhorn, LLC v. Wistron Corporation*, 2:17-cv-711 (E.D. Tex.) (the "Wistron Litigation"), extrinsic evidence cited by Phenix and Defendants in support of their proposed constructions, extrinsic evidence cited by Innolux Corporation, which I understand is a party to *Phenix Longhorn LLC v. Innolux Corporation*, 2:23-cv-478 (E.D. Tex.) (the "Innolux Litigation"), and other documents referred to herein or identified in Appendix 2.

11. Additionally, I have considered information generally available to, and relied upon by, persons of ordinary skill in the art, including well-known engineering principles practiced in the industry. I further relied on my education, experience, and knowledge of basic engineering practices in the industry. I conducted my review from the perspective of a person of ordinary skill in the art ("POSITA" or "POSA") at the time of the invention. My opinions reflect study and consideration of the materials and information and my findings resulting from that study and from my understanding of applicable legal principles described below.

12. I anticipate referring to some of the materials and information, or additional materials and information that comes out during the course of this proceeding (such as by deposition testimony), as well as representative charts, graphs, diagrams, or models that will be

based on such materials and information, to support, summarize, and explain my testimony at the trial.

VI. SUMMARY OF OPINIONS

13. As discussed in detail below, it is my opinion that Defendants' proposed constructions of the disputed claim terms are correct. I have reviewed the constructions proposed by Phenix in this matter, as well as those proposed by Phenix in the Innolux Litigation. In my opinion, Phenix's proposed constructions in this case do not generally represent the meaning of the terms that would be understood by a POSITA (as defined below). By contrast, in my opinion, Defendants' constructions are consistent with the understanding that a person of ordinary skill in the art would reach in view of the plain and ordinary meaning of the terms in light of the specification of the Asserted Patents. I also agree with Defendants that certain disputed claim terms of the '788 patent are indefinite for the reasons stated below.

VII. RELEVANT PRINCIPLES OF LAW

14. I am not a legal expert, and, therefore, offer no opinions of the law. I have been informed, however, of applicable legal principles and applied those principles in this declaration. I will describe my understanding of them.

A. Appropriate Level of Skill in the Art

15. I understand that patent claims are viewed from the perspective of POSITA at the time of the invention, where the "art" is the field of technology to which the patent is related. The purpose of using the viewpoint of a POSITA is for objectivity, and, thus, not the perspective of the inventor, a layperson or a person of extraordinary skill in the art, at the time of the invention.

16. It is my understanding that the relevant factors to consider in determining the level of ordinary skill in the art include at least the following: (1) the type of problems encountered in the art; (2) the prior-art solutions to those problems; (3) the rapidity with which innovations are

made; (4) the sophistication of the technology; and (5) the educational level of workers in the field. In analyzing the proper level of skill in the art of the Asserted Patents, I have considered each of these factors.

17. The Asserted Patents state that they relate to "[a] programmable buffer integrated circuit which can be programmed to output a set of gamma correction reference voltages to be used in LCD displays" and a method for generating a gamma reference voltage for LCD displays. '305 patent at Abstract; *see also* '305 patent at 1:12-15 ("The invention relates generally to the field of liquid crystal displays, and more particularly to TFT flat panel displays and a method of generating a gamma reference voltage").

18. As discussed above regarding my background, I have extensive experience with LCD displays and the development of display technology, the subject matter of the Asserted Patents. I understand that Innolux argued that a POSITA as of June 11, 2003 (the purported priority date of the Asserted Patents) "would have had at least a Bachelor of Science degree in physics, electrical engineering, or the equivalent thereof and three (3) years of experience in circuit design or display technologies. Such a POSA would have had knowledge of integrated circuits, gamma correction, and storage of gamma correction voltage values within memory, and would have understood how to search available literature for relevant publications." Innolux '788 IPR, Petition at 12; *see also* Innolux '305 IPR, Petition at 16. I understand that Phenix, in its Patent Owner Preliminary Response ("POPR") did not dispute Innolux's proposed definition for purposes of its POPR. Innolux '788 IPR, POPR at 2-3; Innolux '305 IPR, POPR at 4. For purposes of this Declaration, I agree with Innolux's definition of a POSITA.

19. My assessment and opinions in the case are based on that perspective of one of ordinary skill in the art at the time of the claimed inventions.

20. I have been informed that Phenix asserts that the Asserted Claims are entitled to a priority date of June 11, 2003. I also understand that this priority date may be disputed by Defendants. Whether the appropriate level of skill in the art is found to be the one that Innolux proposed in the Innolux '788 IPR (or Innolux '305 IPR) or any similar level of skill, I qualified as a person of at least ordinary skill in the art, and although my level of skill is considerably beyond that, I can and did objectively address my opinions on claim construction from the perspective of a POSITA. My opinions in this Declaration would be the same whether the appropriate level of skill in the art is determined to be the level that I propose above, or any similar level of skill.

B. Claim Construction

21. In conducting my analysis of the Asserted Claims, I have applied what I am informed is the legal framework, which I set out below regarding claim construction.

22. It is my understanding that the Court will construe the claims as a matter of law. It is my further understanding that the Court issued a claim construction order in the Wistron Litigation concerning certain claim terms of the '305 Patent. I understand that the parties have agreed to abide by some of the constructions issued by the Court in the Wistron Litigation, but that the parties dispute other constructions from the Wistron Litigation.

23. I understand that the parties have proposed constructions for certain terms in the Asserted Claims of the Asserted Patents. A comparison of these constructions is included in Section IX, below. I reserve the right to offer additional opinions based on the constructions ultimately adopted and communicated by the Court if I prepare and serve a report regarding my opinions on whether the products Phenix has accused of infringing the Asserted Claims actually do infringe the Asserted Claims and/or whether the Asserted Claims are invalid. That report may contain additional opinions, including the application of the plain and ordinary meaning to a person of skill in the art as to certain terms. I do not intend this Declaration to be comprehensive of such

constructions. Rather, the subject matter of this Declaration concerns only the proper constructions for terms the parties have identified for construction in their Patent Local Rule 4-3 Joint Claim Construction Chart and Prehearing Statement.

24. If Phenix changes its apparent interpretation of the claims or offers other interpretations (either explicitly or implicitly) in such a manner as to affect my conclusions, I may supplement or revise my opinions. I also reserve the right to, and may, offer testimony at a hearing on claim construction, and my opinion of how certain words and/or phrases should be construed.

25. I have been instructed by counsel on the law regarding claim construction and patent claims, and I understand that a patent may include two types of claims, independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim or another dependent claim. I understand that a dependent claim includes all of the limitations that it recites in addition to all of the limitations recited in the claim from which it depends.

26. I have been instructed by counsel that claim construction is a matter of law for the arbiter of law to decide. Claim terms should be given their ordinary and customary meaning within the context of the patent in which the terms are used, i.e., the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention in light of what the patent teaches.

27. I understand that claims of a patent are interpreted from the perspective of one of ordinary skill in the art at the time of the invention in light of the intrinsic evidence, which includes the language of the claim itself, the specification of the patent, other claims of the patent (if any) and the relevant prosecution history from the United States Patent and Trademark Office ("USPTO"). Other evidence (such as dictionaries) not in the written record of the patent, and other

extrinsic evidence also may be considered if it is consistent with (not contradictory to) the intrinsic evidence. My understanding is that it is not necessary to rely on extrinsic evidence if the meaning of the claims is clear from the intrinsic evidence. I also understand that, as a general matter, a claim should not be limited to a preferred embodiment. However, in certain cases, the scope of the claims may be limited by a narrow disclosure. I also understand that the full scope of the claims must be supported by the specification. These principles are discussed in more detail below.

28. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a POSITA would have understood disputed claim language to mean. Such sources include the words of the claims themselves, the patent's specification, the prosecution history of the patent (all considered "intrinsic" evidence), and "extrinsic" evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. I understand that *inter partes* review proceedings, including the Wistron IPR, Innolux '305 IPR, and Innolux '788 IPR, are typically treated as intrinsic evidence.

29. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent specification, and the prosecution history.

30. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

31. I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else. In making this determination, the claims, patent specification, and prosecution history are of paramount

importance. Additionally, the specification and prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its own special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope.

32. I understand that the claims of a patent define the scope of the rights conferred by the patent. The claims are required to particularly point out and distinctly claim the subject matter that the patentee regards as their invention. Because the patentee is required to define precisely what they claim their invention to be, it is improper to construe claims in a manner different from the plain and ordinary meaning of the terms used in view of the specification. Accordingly, a claim construction analysis must begin and remain centered on the claim language itself. Additionally, the context in which a term is used in the asserted claim can be highly instructive. Likewise, other claims of the patent in question, both asserted and unasserted, can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims. Differences among claims can also be a useful guide in understanding the meaning of particular claim terms.

33. The specification is the primary basis for construing the claims and provides a safeguard such that correct constructions closely align with the specification. Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim as set forth in the patent itself.

34. I understand that the purpose of the specification is both to teach and to enable those of skill in the art to make and use the invention. The specification must also describe the invention set forth in the claims. In turn, the claims cannot be of broader scope than the invention that is set

forth in the specification. Heavy reliance on a dictionary to determine the meaning of words in a claim, divorced from the intrinsic evidence (such as the specification), risks transforming the meaning of the claim term to the artisan into the meaning of the term in the abstract, out of its particular context, which is the specification.

35. I understand that while intrinsic evidence is of primary importance, extrinsic evidence, e.g., all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. Extrinsic evidence should not be considered, however, divorced from the context of the intrinsic evidence. Evidence beyond the patent specification, prosecution history, and other claims in the patent should not be relied upon unless the claim language is ambiguous in light of these intrinsic sources. Furthermore, while extrinsic evidence can shed useful light on the relevant art, it is less significant than the intrinsic record in determining the legally operative meaning of claim language.

36. I understand that in general, a term or phrase found in the introductory words of the claim, the preamble of the claim, should be construed as a limitation if it recites essential structure or steps, or is necessary to give life, meaning, and vitality to the claim. Conversely, a preamble term or phrase is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention. In making this distinction, one should review the entire patent to gain an understanding of what the inventors claim they actually invented and intended to encompass by the claims.

1. Means-Plus-Function Limitations

37. I understand that claim elements of a patent may be written in what is known as a "means-plus-function" form. I understand that a claim element is in means-plus-function form when it is expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support of the claimed function. I understand the standard to

determine whether a claim is in means-plus-function form is whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for a structure or class of structures. Use of the word "means" in a claim limitation creates a rebuttable presumption that the claim element is written in means-plus-function form. If the word "means" is not used in a claim limitation, there is a rebuttable presumption that a claim element is not written in means-plus-function form. This presumption—that a claim element is not written in means-plus-function form—can be overcome if the claim term fails to recite sufficiently definite structure or else recites function (by use of functional language associated with the claim term) without reciting sufficient structure for performing the recited function. Inspection of the claim is part of the process to (1) make the determination whether a claim term is a means-plus-function term and (2) if a term is a means-plus-function term, determine the function or functions associated with the means-plus-function term.

38. Once it is determined that a claim term is a means-plus-function term, there is a two-step process to construe that term. The first step is to identify the claimed function. I understand that the claimed function is that recited in the claim itself. I further understand that when a means-plus-function term is used in different claims and recites different functions, that the construed functions must be different. That is, different recited functions require different construed functions. The second step is to identify what structure, if any, disclosed in the specification corresponds to the recited function. Structure in the specification qualifies as corresponding structure if, but only if, (1) the intrinsic evidence clearly links or associates that structure with the recited function, and (2) the structure is adequate to perform the recited function. Whether structure disclosed in the specification satisfies either of these requirements is determined from the perspective of a POSITA. If the specification fails to disclose adequate corresponding

structure—either because the specification does not clearly link a structure to the recited function or because a structure linked to the function is not adequate to perform the recited function—the claim is indefinite.

39. I understand that terms determined to be in means-plus-function format are construed to cover the corresponding structure(s) in the specification or their equivalents.

40. I understand that for a means-plus-function term reciting a function carried out on a computer or microprocessor, the only acceptable corresponding structure is an algorithm that can perform the recited function. That is, the structure for a means-plus-function term that recites a function performed by a computer or microprocessor, is an algorithm. The structure is not the computer or microprocessor itself, but rather, a computer or microprocessor programmed with the particular disclosed algorithm making it a special purpose device programmed to carry out the particular function. I understand that there may be narrow exceptions to this rule for functions that can be carried out on any general-purpose computer, such as basic information storage or basic arithmetical computations. My understanding is that such basic functions do not require an algorithm disclosed in the specification. But for any other special-purpose function recited in means-plus-function format, the specification must disclose an algorithm. The algorithm may be disclosed as a figure, in a flowchart, or in words, but the specification must disclose a particular algorithm to a person of skill in the art. Where the specification does not disclose any such algorithm, the claim limitation lacks sufficient disclosed structure, and is therefore indefinite.

C. Indefiniteness

41. I further understand under pre-AIA ("America Invents Act") 35 U.S.C. § 112 ¶ 2 that a patent specification must conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as their invention. A patent claim is invalid for indefiniteness if the claim, read in light of the patent's specification and prosecution

history, fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention. Definiteness is to be evaluated from the perspective of a POSITA, and claims are to be read in light of the patent's specification and prosecution history. Definiteness is to be measured as of the time of the patent application. I understand that it is not enough that it may be possible to ascribe *some* meaning to a patent's claims, and that the zone of uncertainty on what infringes renders a claim indefinite where the claim read in light of the specification and the prosecution history from the perspective of ordinary skill in the art does not inform with reasonable certainty what is or is not an infringement.

42. Again, I understand that the pre-AIA version of 35 U.S.C. § 112 applies to the Asserted Patents because they were effectively filed before March 16, 2013.

43. I understand that where a claim term is ambiguous and does not have a plain and ordinary meaning to a person of ordinary skill in the art, the ambiguity does not necessarily render a claim term indefinite. In particular, I understand that such ambiguity in the scope of a claim should be resolved, if possible, by interpreting the term in light of the intrinsic record.

44. I understand that a claim term in a patent may be indefinite where it lacks antecedent basis, and thus, is unclear. For example, the lack of clarity could arise where a claim refers to "said lever" or "the lever," (using words "said" or "the" to signal that the term had been previously introduced) where the claim contains no earlier recitation or limitation of a lever and where it would be unclear as to what element the limitation was making reference.

45. I understand that indefiniteness must be proven by clear and convincing evidence and my opinions in this declaration reflect this understanding.

VIII. BACKGROUND OF THE ASSERTED PATENTS

A. The Specification of the Asserted Patents

46. I understand that the Asserted Patents, the '305 patent the '788 patent, share the same specification, as the '788 patent is a continuation of the '305 patent. As such, any citations to either of the Asserted Patents will reference the '305 patent, regardless of whether the discussion pertains to the '305 patent or the '788 patent.

B. Summary of the '305 Patent

47. The '305 patent purports to claim a programmable buffer integrated circuit designed to output a set of gamma correction reference voltages specifically for use in liquid crystal displays ("LCDs"). The central problem to be purportedly solved by the '305 patent is the need for an automated, cost-effective solution to gamma correction that avoids the complexities and expenses associated with digital approaches. The patent describes an analog system that utilizes analog non-volatile memory to store gamma correction values, allowing for programmable gamma correction. '305 patent at 2:16-28. As such, the '305 patent provides for an entirely analog device for gamma correction, enabling gamma adjustment tailored to specific display requirements.

48. Figure 3 illustrates one embodiment of a gamma controller. The gamma controller 300 shows programming engine or interface 300 (red), a mux (i.e., multiplexer) 320 (green), programmable analog floating gate memory cells 330 through 337 (blue), and drivers 340 through 347 (yellow). *Id*. at 3:50-52. The programming engine is connected to the mux and includes an Analog Input used to establish the reference voltage level, along with a Read/Write ("R/W") control signal for the gamma reference controller. *Id*. at 3:52-56. The mux facilitates the connection of signals from the programming engine to any of the programmable analog floating

gate memory cells, based on three address inputs (A_0, A_1, and A_2), highlighting the analog nature of the system's operation. *Id*. at 3:56-4:2.

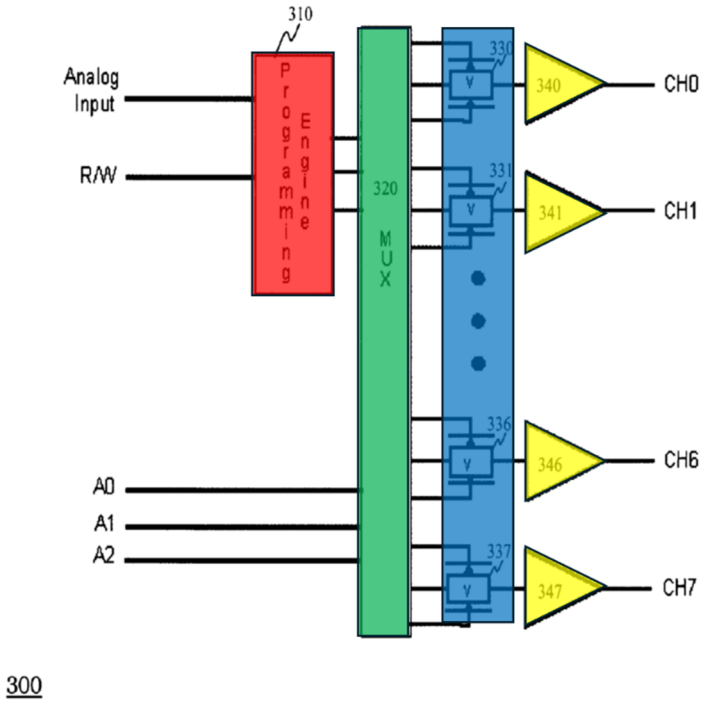


FIG. 3

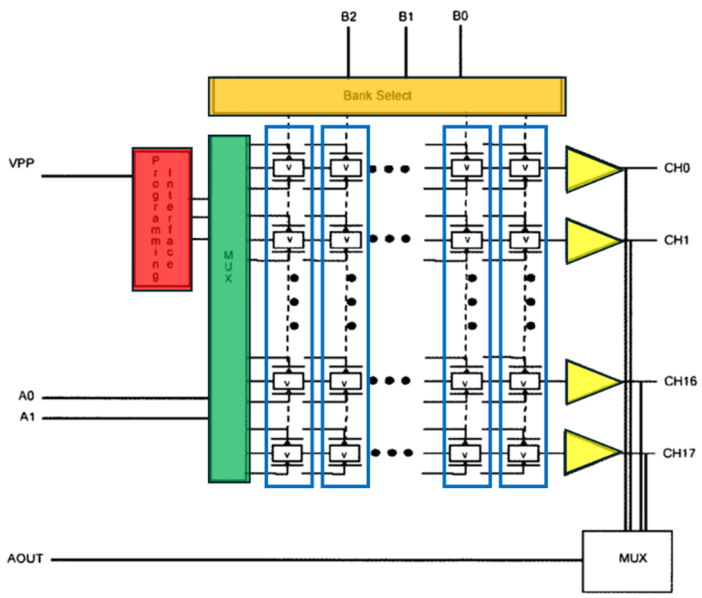
49. Figure 3 further illustrates that each output (channel 0 (CH0) through channel 6 (C6)) is "internally connected to an analog storage cell which can be written with analog values," each output designed to directly drive the reference voltage inputs of the source driver integrated circuit. *Id*. at 4:4-9. In addition, Figure 3 further highlights the analog nature of the system as there is an internal voltage multiplier which produces an output voltage ranging from 0 volts up to at least 16 volts by multiplying an analog value by a multiplication factor M. *Id*. at 4:9-11.

50. Figure 6 shows an alternative embodiment. In this embodiment, the '305 patent describes an integrated circuit identified as the AG1818, which is "a programmable gamma reference generator with integrated output buffers to directly drive" source driver inputs of a

display. *Id*. at 5:30-33. Compared to the embodiment disclosed in Figure 3, the AG1818 purports to organize the programmable analog floating gate memory cells into multiple banks (blue boxes) where each bank contains a predetermined gamma reference voltage data for different display conditions. *Id*. at 5:49-58. The banks of programmable analog floating gate memory cells storing the aforementioned predetermined analog gamma reference voltage data can be selected through the address inputs B_0 through B_2, which are inputs to a Bank Select module (orange). *Id*. at 5:52-53. Similar to the embodiment of Figure 3, each out output of the AG1818 (CH0 through CH17) is also "internally connected to an analog nonvolatile storage cell, which can be written with 1,024 analog values, providing . . . better than 15 mV resolution." *Id*. at 5:40-43.

FIG. 6

BLOCK DIAGRAM (AG1818)



C. Summary of the '788 Patent

51. The '788 patent purports to claim a method for calibrating a liquid crystal display to a desired gamma curve to compensate for panel to panel manufacturing variations. *Id*. at

Abstract. The '788 patent describes incorporating a programming interface that enables the buffer outputs of each panel to be set to specific values during manufacturing and testing, allows multiple sets of gamma values to be stored for optimized correction curves tailored to different needs, and supports automated assembly, automated testing and adjustment, a more compact design, lower power consumption, and reprogrammable, non-volatile settings. *Id*. at 2:23-33.

52. Figure 2 presents a gamma reference circuit implementation employing gamma reference controllers (light green), TFT panel (purple), source drivers (pink), and a programming interface (brown). The programming interface includes a shared "Analog Input" ("A_{IN}") for setting the reference voltage, three address lines (A_0, A_1, and A_2) to establish which reference level is being programmed, and separate read/write ("R/W") control signals for each of gamma reference controllers present on a board. *Id*. at 3:7-13.

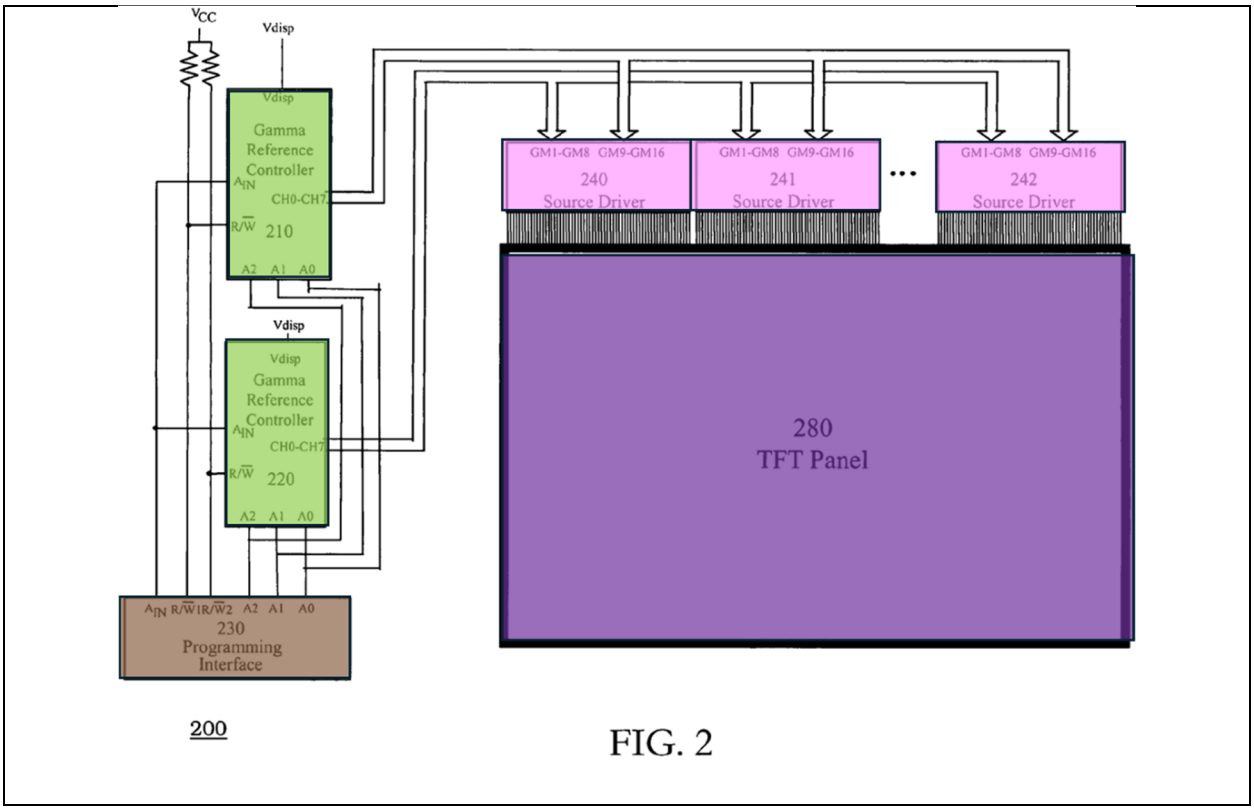


FIG. 2

53. The '788 patent states that the "programming operation is accomplished by first selecting the output or channel of the device to be programmed with the A_2-A_0 inputs." *Id*. at 3:17-

19. Once the programming interface selects its desired output, the programming interface sets the R/W terminal to low, thereby configuring the gamma reference circuit to enter what the patent refers to as the "Tracking Mode," during which the output of the chosen channel follows the voltage applied to the Analog Input terminal. *Id*. at 3:19-22. The programming interface functions so that, after varying the Analog Input terminal to the desired analog voltage value for a specific channel, the R/W terminal is set high such that this value is stored in the analog nonvolatile memory for the output channel selected by the address inputs. *Id*. at 3:25-29.

54. The invention further describes that automated panel testing for each panel can be accomplished using optical sensors that provide feedback to the gamma correction circuitry such that once the sensors have calibrated the gamma reference voltages to achieve the desired display brightness, these values can be saved, allowing different application scenario to be "pretested and stored." *Id*. at 7:20-28. Additionally, a sensor can be included with the display to detect environmental factors such as temperature or lighting, enabling the system to select the appropriate gamma settings based on current conditions. *Id*. at 7:28-32.

D. File History of the '305 Patent

55. The '305 patent originally issued on June 19, 2007 from U.S. Patent Application No. 10/746,333 (the "'333 application") filed on December 23, 2003. As indicated on the face of the '305 patent, the '333 application claims priority to U.S. Provisional Patent Serial No. 60/477,680 (the "'680 application"), filed on June 11, 2003.

56. A non-final office action was issued on September 6, 2006 rejecting all claims. Claims 1-7, 12, and 16-22 were rejected under 35 U.S.C. § 112, second paragraph; claim 1, 2, and 5 were rejected as anticipated by U.S. Patent No. 6,373,478 B1 ("Steffensmeier"); claim 8 was rejected as obvious over U.S. Patent No. 5,593,934 ("Liaw"); and claims 9-13 were rejected as

obvious over Liaw in view of U.S. Patent No. 7,038,721 ("Stessen"). Phenix_AUO_Hisense_0000310-319 (Examiner's Non-Final Rejection).

57. In particular, and as it pertains to the rejection of claims 1, 2, and 5, the Examiner cited to Steffensmeier to point out that claim 1 was in part rejected because Steffensmeier taught an integrated circuit for producing voltage signals where the plurality of non-volatile storage cells was disclosed and equated to "analog memory devices 50." Phenix_AUO_Hisense_0000314. Additionally, the Examiner stated that circuits for programming coupled to a multiplexer for "addressing and programming said storage cells" was also disclosed via "device 54 [as] [it] provides an analog voltage to one of the analog memory device 50 while control circuit 56 controls the reception and provision of signals by and from analog devices 50." *Id.*

58. Thus, my understanding is that the Examiner recognized that the '305 patent is directed to an analog solution through the identification of Steffensmeier's analog memory device and analog voltage signaling as anticipating the claim 1 of the '305 patent. My understanding (discussed in additional detail below) is further supported by the interpretation by the Examiner during the prosecution of the '305 patent, confirming that the '305 patent is directed to an analog implementation of gamma correction rather than a digital one.

59. The Patent Owner ("PO"), in order to resolve the rejections based on Steffensmeier, amended claim 1 by including the allowable subject matter of dependent claim 3, eliminating the insufficient antecedent issue of claim 4, and the indefinite issues of claim 1, thereby receiving a Notice of Allowance on February 21, 2007. Phenix_AUO_Hisense_0000296-297, Phenix_AUO_Hisense_0000303-304 (Applicant's Response to Examiner's Non-Final Rejection); *see also* Phenix_AUO_Hisense_0000284-287 (Notice of Allowability). I understand that the Examiner, in the Notice of Allowance stated that "[i]ndependent claim 1 identifies, inter alia, the

uniquely distinct features 'wherein said non-volatile storage cells are organized into one or more banks of cells where in each bank contains a predetermined gamma reference voltage signal display condition; and means to switch between the banks based on one or more external signals is provided on said integrated circuit." Phenix_AUO_Hisense_0000286 (Notice of Allowability). Further, I understand that the Examiner concluded that Steffensmeier "does not teach or suggest" the above claimed feature as Steffensmeier teaches a "column driver for providing gray scale voltage signals to column lines" where the "column driver includes analog memory devices for data storage . . . , a multiplexer bus circuit for addressing one of the analog memory devices, and buffers for buffering outputs of the analog memory devices." Phenix_AUO_Hisense_0000287 (Notice of Allowability).

60. I understand that two petitions for *Inter Partes* Review ("IPR") of the '305 patent have been filed. I understand that Wistron Corporation filed the Wistron IPR in 2018 and that Innolux filed the Innolux '305 IPR in 2025. I understand that the Wistron IPR was not instituted. *See* Wistron IPR, Institution Decision (Jan. 24, 2019). I understand that the Patent Trial and Appeals Board ("PTAB") has not issued an institution decision in the Innolux '305 IPR as of the date of this Declaration.

E. File History of '788 Patent

61. The '788 patent originally issued on July 7, 2009 from U.S. Patent Application No. 11/743,014 (the "'014 application"), filed on May 1, 2007. As indicated on the face of the '788 patent, the '014 application is a continuation of the '333 application (which issued as the '305 patent) and claims priority to the '680 application.

62. A non-final office action was issued on July 22, 2008 rejecting the original claims as obvious over Liaw where the Examiner stated in relevant part that while Liaw did not teach that the "memory 21 is non-volatile," that "one of ordinary skill in the part would recognize that LCD

has a non-uniform gamma characteristics that would require gamma correction and that a non-volatile memory would serve to avoid the need to setting gamma reference voltages every time the display is powered up." Phenix_AUO_Hisense_0000504-506 (Examiner's Non-Final Rejection). In response, the PO did not make any substantive amendments to the original claims, however, the PO argued that several claim limitations were not disclosed in Liaw. For example, the PO stated that a "method for calibrating a liquid display," "compensating for panel-to-panel manufacturing variations," the memory is "electrically reprogrammable and non-volatile," and the gamma reference voltage levels are applied on the columns of a display. Phenix_AUO_Hisense_0000485-486 (Applicant's Response to Examiner's Non-Final Rejection). The PO further argued that Liaw does not disclose a non-volatile memory asserting that it would not have been obvious for a person having ordinary skill in the art to use non-volatile memory in light of Liaw. Phenix_AUO_Hisense_0000486 (Applicant's Response to Examiner's Non-Final Rejection).

63. A Notice of Allowance was issued by the Examiner on March 5, 2009 without comment on the reasons for allowance. Phenix_AUO_Hisense_0000458-460 (Notice of Allowance and Fee(s) Due).

IX. CLAIM CONSTRUCTION

64. I understand that the parties are submitting a Joint Claim Construction and Prehearing Statement on the date that this Declaration is being submitted. I also understand that the parties exchanged an identification of preliminary claim constructions and extrinsic evidence. Those documents are attached to my Declaration as Appendices 3 and 4.

A. Agreed Constructions

65. I understand that the parties have agreed upon the following constructions for certain terms of the Asserted Patents:

#	Claim Term	Agreed Construction
1	An integrated circuit for producing voltage signals on a plurality of outputs comprising:	Limitation reciting one integrated circuit
2	Circuits for programming	Plain and ordinary meaning
3	Programming said storage cells	Writing data to a storage cell
4	Drivers	Buffers or amplifiers
5	Predetermined gamma reference voltage signal display condition	A display condition established by the predetermined gamma reference voltage signals based on the application that is being displayed, external environment such as temperature and ambient light, or the personal preference of the user
6	Means to switch between the banks based on one or more external signals	**Function:** switching between the banks based on one or more external signals **Structure:** '305 patent at 5:50-6:21; Fig. 4A (B0-B2); Fig. 4B (pins 20, 22, 23); Fig. 5 (Tdamp); Fig. 6 (Bank Select, B0, B1, B2)
7	High voltage programming means	**Function:** programming the non-volatile storage cells using a high voltage signal; **Structure:** (1) (a) a Program Interface, (b) a Vpp input that is used to select the programming mode, (c) the Vpp input also providing the high voltage pulses used during programming of an individual cell, and (d) address inputs A0 and A1 / bank inputs B0, B1, B2 used to select the location being programmed; as described at '305 Patent 6:22-26, Figs. 4A, 4B, 5, or 6 **and/or** (2) (a) a Program Interface, (b) a Vpp input, address inputs A0 and A1, and bank inputs B0, B1, B2 that are used to select the programming mode, (c) the Vpp input also providing the high voltage pulses used during programming of an the [sic] individual cell, and (d) address inputs A0 and A1 and bank inputs B0, B1, B2 used to select the location being programmed; as described at '305 Patent 6:37-53, Figs. 4A, 4B, 5, and 6

#	Claim Term	Agreed Construction
8	A method of calibrating a liquid crystal display to a desired gamma curve to compensate for panel-to-panel manufacturing variations comprising the steps:	Preamble is limiting

B. Disputed Constructions

66. I understand that the parties have proposed constructions on the following terms where there is disagreement on the proposed construction. I have only been asked to opine about some of the terms where the parties disagree on the proposed construction. Those terms are discussed in detail below. For the remaining terms where there is a disagreement on the proposed construction, I have not been asked to analyze these terms or analyze the parties' proposed construction of these terms.

#	Claim Term	Defendants' Construction	Phenix's Construction
1	Non-volatile storage cells	Analog memory cells which retain stored data even when power is removed	Memory cells which retain data even when power is removed
2	Coupled to	Indirectly or directly linked	No construction necessary; plain and ordinary meaning
3	Multiplexer for addressing and programming said storage cells	One or more circuits, excluding an I2C serial bus that couple (1) one input (or one set of inputs) to one of many outputs (or one set of many sets of outputs) or (2) one of many inputs (or one	No construction necessary; plain and ordinary meaning[1]

[1] I understand that Phenix's proposed construction for the term multiplexer is "one or more circuits that selectively couple (1) one input (or one set of inputs) to one of many outputs (or one set of many sets of outputs) or (2) one of many inputs (or one set of many sets of inputs) to one output (or one set of outputs)," which is the construction Phenix and Wistron agreed to in the Wistron Litigation.

#	Claim Term	Defendants' Construction	Phenix's Construction
		set of many sets of inputs) to one output (or one set of outputs)	
4	Connected to	Directly and/or physically linked	No construction necessary; plain and ordinary meaning
5	Bank(s)	Contiguous section(s) of addressable computer memory arranged in n by m matrix format	No construction necessary; plain and ordinary meaning
6	Gamma reference control capability	Indefinite	No construction necessary; plain and ordinary meaning
7	Control circuit	Indefinite	No construction necessary; plain and ordinary meaning
8	Means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor	Indefinite	Function: executing a predetermined algorithm Structure: programming interface
9	Predetermined algorithm	Indefinite	No construction necessary; plain and ordinary meaning
10	Gamma reference voltage levels	An analog voltage(s) stored in an analog storage cell	No construction necessary; plain and ordinary meaning

C. Construction of Disputed Terms

67. I have been asked to opine on the construction of six disputed claim terms: (1) non-volatile storage cells; (2) gamma reference control capability; (3) control circuit; (4) means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor; (5) predetermined algorithm; and (6) gamma reference voltage levels. Of these claim terms, the term "non-volatile storage cells" appears in claim 1 of the '305 patent. The remaining claim terms that I have been asked to opine on appear in claim 1 of the '788 patent.

68. I understand that Defendants identify two terms—"control circuit" and "means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor"—that should be construed as means-plus-function terms. I address these two terms first in my opinions below, followed by the remaining terms of the '788 patent. Finally, I address the term "non-volatile storage cells" that appears in claim 1 of the '305 patent.

69. As an initial matter, in my opinion and as further explained below, the claim terms "control circuit" and "means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor" should be construed as means-plus-function terms. To support my opinion that these terms are means-plus-function terms, my analysis will first show that (1) the term-at-issue is not the name of a structure or class of structures that a POSITA would be familiar with; (2) that the Asserted Claims do not provide structure for each claim term that is capable of performing the recited functions of that claim term; and (3) that the specification does not contain an express definition of the claim term (in a lexicographical sense) or a description of structure sufficient to show that the claim term was known in the art as of the alleged priority date of the Asserted Patents.

70. After establishing why, in my opinion, the terms should be construed as means-plus-function terms, I will first show what I believe to be the function(s) of the claim term as

recited in the Asserted Claims. Second, I will describe my opinion regarding whether the specification describes adequate structure to perform the recited function. If the specification does not describe adequate structure to perform the recited function, in my opinion, the claim term is indefinite.

1. Control Circuit

"Control circuit" '788 patent, claim 1	Subject to 35 U.S.C. § 112 ¶ 6 **Function**: varying gamma reference voltage levels on columns of a display **Structure**: None (indefinite)

71. I understand that Defendants contend that the term "control circuit" is a means-plus-function claim term but that it is indefinite because there is no corresponding structure to perform the function in the specification.

72. I agree with Defendants. In my opinion, the term "control circuit" should be construed as a means-plus-function term because the Asserted Claims do not recite a sufficient structure for performing the recited function. The term "control circuit" is also indefinite because there is not a sufficient structure described in the specification that performs the function of "varying gamma reference voltage levels on columns of a display."

a. The Term "Control Circuit" Should Be Construed As A Means-Plus-Function Term

73. In my opinion, the term "control circuit" is a means-plus-function term. As discussed in more detail below, I reach that conclusion on the basis that (1) the term "control circuit" represents an extremely broad class of structures without any sufficient bounds; (2) the full claim language in which the phrase "control circuit" appears does not recite structure for

"control circuit" that is capable of performing the function recited in the claim; and (3) the specification, to the extent that it describes any structure at all, does not define "control circuit" as those structures.

74. To a POSITA, the term "control circuit" is a term generally known in the art. However, it represents an extremely broad structure or class of structures and without additional details or context, a POSITA would be unable to determine a particular structure, composition, or arrangement intended in the Asserted Patents. For example, a "control circuit" could be a wall switch or a complex circuit that manages inputs to a TV. The breadth of the term leaves substantial ambiguity regarding the precise nature and boundaries of the "circuit" being claimed and how or what it "controls." To a POSITA, the term "control circuit" is a purely functional term that describes the intended result of "control," without connoting any definite structure for how that "control" is achieved. In other words, the term "control circuit" is a generic term, and "control" is simply the function that a "circuit" is intended to perform.

75. Claim 1 of the '788 patent does not define any structure for the recited "control circuit" as claim 1 simply states that the "control circuit" "var[ies] gamma reference voltage level on columns of said display, wherein said control circuit is separate from said display." This does not provide any pertinent information about the structure of a "control circuit" and a POSITA would not understand the requirement that the "control circuit" being separate from the display to impart any structural meaning to the term "control circuit."

76. The term "control circuit" is also not defined in the specification of the Asserted Patents. Specifically, there is no disclosure in the specification where the inventors defined the term "control circuit" in a lexicographical sense. Nor does the specification suggest that "control circuits" were known in the art as a particular structure or class of structures. In fact, the term

"control circuit" appears twice in the '788 patent, recited only in claim 1, where it is described as "varying gamma reference voltage levels on columns of said display by a control circuit, wherein said control circuit is separate from said display," but the specification provides no explanation or detail as to what the inventors intended the "control circuit" to mean. Most notably, the specification does not disclose any specific circuitry, components, architecture, or structural implementation that would constitute the claimed "control circuit." Because there is a complete absence of disclosure regarding the structure of the "control circuit," a POSITA would not be able to determine what apparatus or structure performs the claimed function of "varying gamma reference voltage levels." This lack of corresponding structure in the specification strongly suggests that the term should be construed as a means-plus-function limitation, even though it does not use the phrase "means for," because the term fails to recite sufficiently definite structure and instead describes a function without providing adequate structural detail for performing that function.

b. The Specification Does Not Identify A Corresponding Structure To Perform The Function Of A Control Circuit

77. As discussed above, it is my opinion that the term "control circuit" is a means-plus-function term. Therefore, I will determine what "function" in the term "control circuit" performs in the Asserted Claims and what structure(s), if any, is disclosed in the specification that can perform the recited "function."

78. The function of the "control circuit" is recited in asserted claim 1 of the '788 patent. Claim 1 of the '788 patent recites "varying gamma reference voltage levels on columns of said display by a control circuit, wherein said control circuit is separate from said display." It follows that the properly understood function of the "control circuit" is to "vary[] gamma reference voltage levels on columns of [a] display."

79. As discussed above, the only mention of a "control circuit" in the specification resides in the actual claim limitation just recited. That is, other than claim 1 of the '788 patent, the term "control circuit" is absent from the entire specification. Even the functional term "varying" appears only three times in the specification: once in asserted claim 1, once in claim 5, and once in the description of Figure 2.

80. Figure 2, as discussed below, describes a "gamma reference circuit implementation employing gamma reference controllers, 210, and 220, for a TFT panel 280" and also includes a "Programming Interface 230 [which] comprises a common Analog Input (A_{IN}) used to set the reference voltage." '305 patent at 2:62-3:9. The manner in which this is accomplished is a "desired voltage is found by varying the Analog Input for a particular channel." *Id*. at 3:25-26. However, this passage simply describes manipulating an input during a programming operation, it does not disclose any specific structure that performs the claimed function of "varying gamma reference voltage levels on columns of said display."

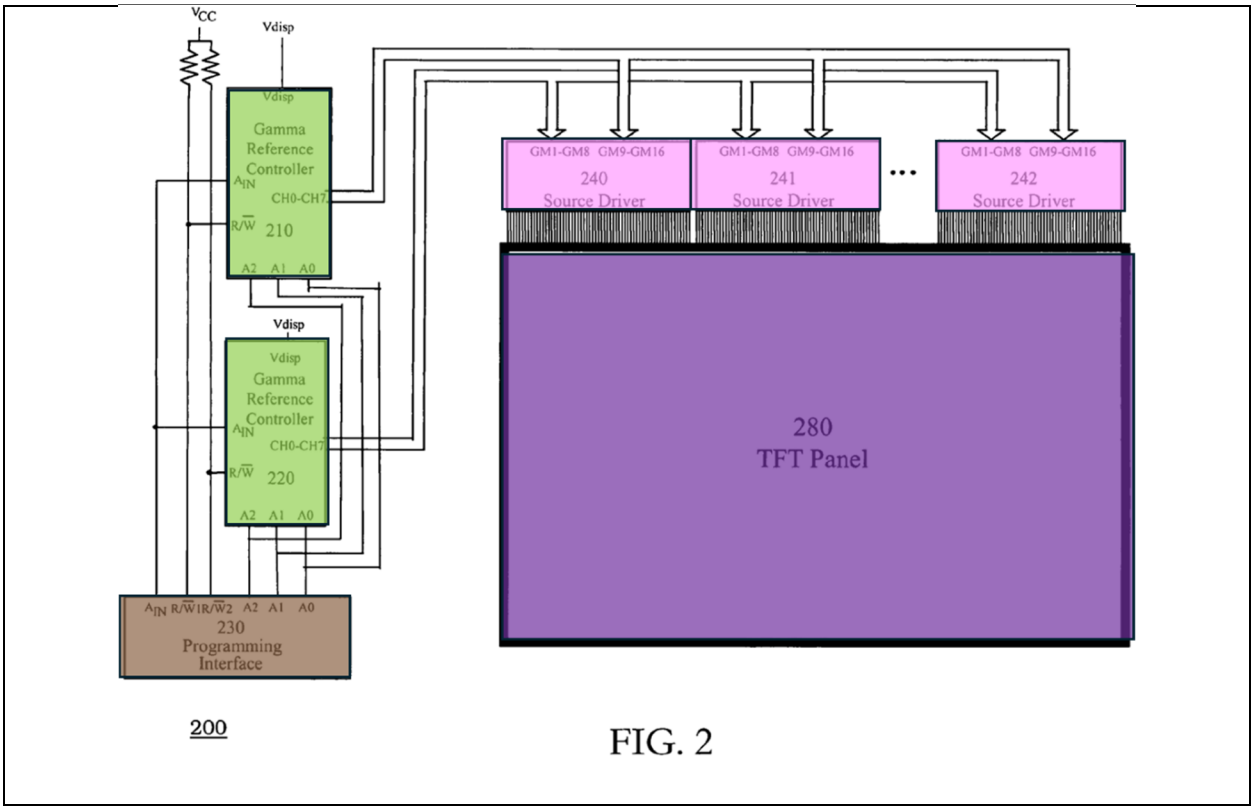


FIG. 2

81. While the specification discloses that a programming interface 230 plays a role in varying the voltage applied to its Analog Input terminal, it nonetheless fails to provide any structural details whatsoever about what constitutes the claimed "control circuit." There is no disclosure of circuitry, components, architecture, or any specific hardware that would perform the function of varying gamma reference voltage levels. The specification treats the "control circuit" as essentially a black box, with no information about its internal structure or composition. Without such disclosure, a POSITA would be unable to identify what structure performs the claimed function.

82. Further, the embodiment disclosed in Figure 3, in my opinion, does not disclose any specific structure that performs the claimed function of "varying gamma reference voltage levels on columns of said display." Like the embodiment of Figure 2 which presents a programming interface, Figure 3 provides a block diagram illustrating one embodiment of the gamma reference controllers described in Figure 2. The gamma reference controller also includes

a programming engine 310 that includes an Analog Input terminal "used to set the reference voltage level." *Id*. at 3:49-54.

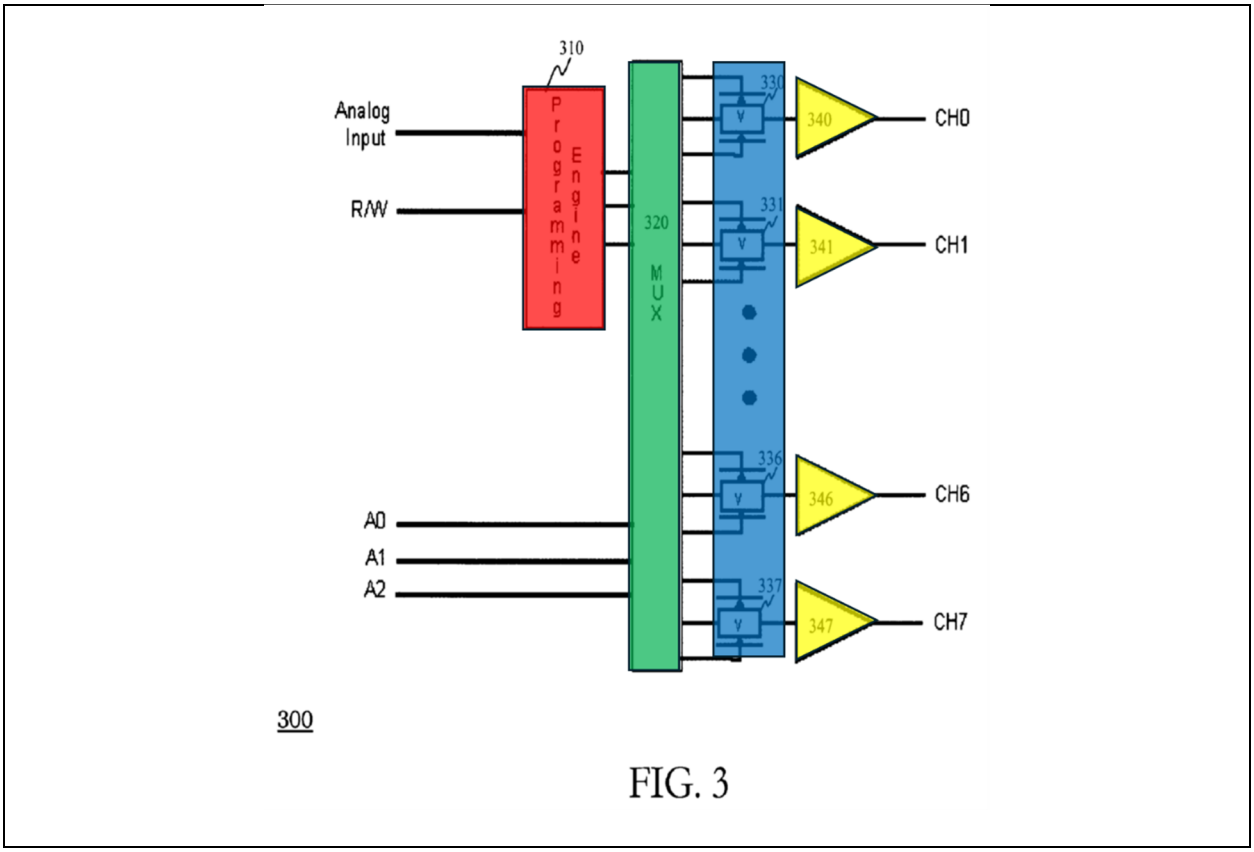


FIG. 3

83. In addition, the gamma reference controller of Figure 2 has two distinct modes, a "read" mode and a "track and write cycle" mode. During read mode, "all channels continuously output their corresponding stored voltage" and during the track and write cycle mode, the "addressed channel now outputs a voltage which is equal to the voltage applied to the Vin pin, multiplied by the voltage multiplication factor M." *Id*. at 4:21-26.

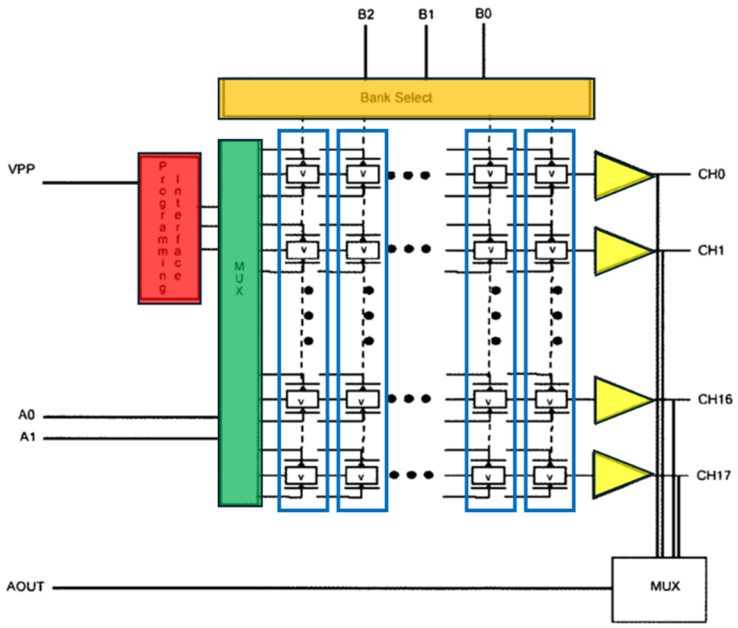
84. In my opinion, neither of these operations helps define a structure for a "control circuit" that performs the function of "varying gamma reference voltage levels on columns of said display." Rather, the programming engine 310 is used to program analog reference voltage values that are then stored in their respective programmable analog floating gate memory cells. Further, Figure 3 and its corresponding description do not provide any structural details about the

programming engine 310. It is described exclusively in terms of its inputs and outputs without any disclosure regarding its internal architecture or components. A POSITA would not be able to ascertain what specific circuitry constitutes a programming engine or how such circuitry could perform the function of "varying gamma reference voltage levels on columns of said display."

85. The AG1818 shown in Figure 6 also does not disclose any structure representing a "control circuit" that performs the claimed function of "varying gamma reference voltage levels on columns of said display" for the same reasons I've discussed above regarding the embodiments of Figures 2 and 3.

FIG. 6

BLOCK DIAGRAM (AG1818)



86. According to the specification, the AG1818 is a "programmable gamma reference generator with integrated output buffers to directly drive the source driver inputs of a display." *Id.* at 5:30-33. The AG1818's programming interface allows for a device to be "programmed in-situ . . . or [to] adjust the gamma reference voltages of an individual display." *Id.* at 6:22-25. In

addition, the programming interface of the AG1818 includes four signals, including V_{PP}, a "high voltage input used to select the programming mode and also provides high voltage pulses used to program individual cells." *Id*. at 6:27-30.

87. The specification also mentions that theAG1818 has an alternative method for programming the analog nonvolatile storage cells. The process involves placing the AG1818 in "Program Mode" by addressing a particular bank through a sequence of address inputs and pulsing the V_{PP} terminal to latch the bank address. *Id*. at 6:37-42. Next, the specific "cell to be programmed in the selected bank is addressed" using another sequence of inputs, followed by pulsing V_{PP} again. *Id*. at 6:42-44. The selected storage cell is then programmed by "pulsing V_{PP} with adjustable voltage pulses between approximately 8 and 14 volts." *Id*. at 6:45-47. Once the cell reaches "the desired voltage level," the device is returned to read mode via a final sequence of address inputs and V_{PP} pulsing. *Id*. at 6:47-50.

88. In my opinion, neither method of programming the analog nonvolatile storage cells through the use of the programming interface constitutes a "control circuit" whose function is "varying gamma reference voltage levels on columns of said display." The programming interface of the AG1818 is used primarily to initially program analog reference voltage values that are then stored in analog nonvolatile memory cells. As with the programming interface of Figure 2 and programming engine of Figure 3, here too the specification provides no structural details about the internal composition of the AG1818's programming interface beyond identifying and relying on its input/output pin designations. Without disclosure of specific circuitry, components, or architecture that would allow for the "varying of gamma reference voltage levels on columns of said display," a POSITA would have no guidance as to what structure corresponds to the claimed "control circuit."

89. Finally, the specification mentions that "[r]eal time monitoring of the cell voltage level is accomplished through the AOUT pin which reflects the cell voltage as it is in the output buffer which is the voltage which will be applied to the display column." *Id.* at 6:58-61. The specification continues that "[i]ndependent of what voltage actually is stored in the cell the AOUT pin gives the ability for closed loop programming such that a precise gamma reference voltage is provided to a specific column." *Id.* at 6:63-67. The discussion of the A*OUT* pin in the specification, however, does not provide a POSITA any structural details or guidance as to what structure varies gamma reference voltage levels on the column of a display. Instead, the AOUT pin, which a POSITA would understand is a pin and not a circuit, is described as a countermeasure to the "vagaries of the design and fabrication process." *Id.* at 6:61-63.

90. This complete absence of structural disclosure renders the term indefinite under 35 U.S.C. § 112, paragraph 6, as there is simply no guidance in the specification regarding what structure corresponds to the claimed "control circuit."

2. Means For Executing A Predetermined Algorithm According To A Predetermined Criteria And Data Sensed By Said At Least One Sensor

"Means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor" '788 patent, claim 1	Subject to 35 U.S.C. § 112 ¶ 6 **Function**: executing a predetermined algorithm according to predetermined criteria and data sensed by said at least one sensor to achieve the desired gamma curve **Structure**: None (indefinite)

91. I understand that both Plaintiff and Defendants contend that the term "means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said

at least one sensor" is a means-plus-function claim term. However, Defendants contend that it is indefinite because there is no corresponding structure to perform the function in the specification.

92. I agree with Defendants. In my opinion, the term "means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor" should be construed as a means-plus-function term because the Asserted Claims do not recite sufficient structure for performing the recited function, and, as discussed below, the specification does not disclose a corresponding structure, rendering the term indefinite.

a. The Term "Means For Executing A Predetermined Algorithm According To A Predetermined Criteria And Data Sensed By Said At Least One Sensor" Should Be Construed As A Means-Plus-Function Term

93. As an initial matter, I understand that under 35 U.S.C. § 112, paragraph 6 (pre-AIA), there exists a rebuttable presumption that a claim limitation is to be treated as a means-plus-function limitations if the claim limitation employs the term "means" in connection with a stated function.

94. As mentioned above, I understand that that all parties agree that this term uses the word "means" and that both parties agree that this term is governed by 35 U.S.C. § 112 paragraph 6 (pre-AIA). However, in my opinion, while the term "means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor," uses the word "means" and recites a function, it does not recite sufficient structure for performing the function. As such, the presumption that § 112, paragraph 6 applies (as I understand it) is not rebutted.

95. Accordingly, the term should be construed as a means-plus-function term under § 112, paragraph 6. The function recited by the claim is "executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor."

b. The Specification Does Not Identify A Corresponding Structure To Perform The Function Of The Means For Executing A Predetermined Algorithm…

96. As discussed above, it is my opinion that the term "means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor" is a means-plus-function term. Therefore, I will determine what "function" in the term performs in the Asserted Claim and what structure(s), if any, is disclosed in the specification that perform the recited "function."

97. The function of the term is recited in asserted claim 1 of the '788 patent. Claim 1 of the '788 patent recites a means for performing the function of "executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor." However, claim 1 does not provide any disclosure or suggestion of what structure performs this function. Hence, I understand that I must look to the specification to identify if any structure performs this function.

98. As discussed previously, Figure 2 describes a gamma reference circuit implementation which utilizes gamma reference controllers for a TFT panel as well as a "Programming Interface 230 [which] comprises a common Analog Input (A_{IN}) used to set the reference voltage." '305 patent at 2:62-3:9. However, this programming interface 230 does not perform the function of "executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor." Instead, the programming interface 230, according to the specification, is being described purely as an interface for setting gamma reference voltages into analog nonvolatile memory cells.

99. For example, the specification states that during normal operation, the "R/W pin is pulled High and the reference voltage outputs will reflect the value last programmed into the nonvolatile memory cells." *Id*. at 3:14-16. Also, "[o]nce a desired voltage is found by varying the

Analog Input for a particular channel, the R/W signal is driven high and the value on the Analog Input is written into the nonvolatile memory." *Id*. at 3:25-29. Thus, the programming interface selects which output channel to program to a specific voltage value, it does not execute any algorithm based on sensor data or "predetermined criteria."

100. Notably, the embodiment of Figure 2 and its corresponding description contain no mention of any sensor, let alone a structure that executes an algorithm based on sensor data or any "predetermined criteria." The gamma reference controllers and programming interface are described solely in terms of their ability to store and output analog voltage values, not in terms of executing algorithms based on sensor input(s).

101. Further, Figure 3 discloses a block diagram illustrating one embodiment of the gamma reference controllers disclosed in Figure 2. However, after analyzing Figure 3 and its corresponding description, I find no disclosure of any structure that performs the claimed function of "executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor."

102. The gamma reference controller in Figure 3 explains that the programming engine 310 which is "coupled to the mux, comprises an Analog Input which will be used to set the reference voltage level." *Id*. at 3:50-55. This programming engine is designed for programming analog voltage values into the programmable analog floating gate memory cells, not for executing algorithms based on sensor data or predetermined criteria. Like the embodiment disclosed in Figure 2, any structure for receiving sensor data is absent, including any structure for executing a predetermined algorithm based on measured sensor data and predetermined criteria.

103. The AG1818 of Figure 6 also does not disclose any structure that performs the claimed function of "executing a predetermined algorithm according to a predetermined criteria

and data sensed by said at least one sensor" for the same reasons I've discussed above regarding the embodiments of Figures 2 and 3.

104. According to the specification, the AG1818 is a "programmable gamma reference generator with integrated output buffers to directly drive the source driver inputs of a display." *Id*. at 5:30-33. The AG1818's programming interface allows for a device to be "programmed in-situ . . . or [to] adjust the gamma reference voltages of an individual display." *Id*. at 6:22-25. In addition, the programming interface of the AG1818 includes four signals, including V_{PP}, a "high voltage input used to select the programming mode and also provides high voltage pulses used to program individual cells." *Id*. at 6:27-30.

105. In my opinion, the programming interface of the AG1818 is not a structure that performs the claimed function as its sole purpose. Rather, and as described in the specification, the programming interface facilitates programming analog voltage values into analog nonvolatile memory cells. As I mentioned above, the specification is clear that the programming interface provides signals to "select the programming mode" and "program the individual cells." Nothing in the description of the AG1818 suggests that the programming interface executes an algorithm, let alone one based on predetermined criteria and sensor data. The function of the programming interface is different from the claimed function—it simply enables the writing of analog voltage values to analog memory, not the execution of predetermined algorithm(s).

106. The specification further mentions that a "PC based programming interface is available for prototyping and gamma optimization" where displaying "optimization algorithms may be located in such a PC." *Id*. at 7:13-17. But the specification does not describe how this PC utilizes data output by any sensor, or what predetermined criteria, if any, is stored on the PC.

107. Each of the embodiments discussed above also lack a sensor. While the specification does mention that "[a]utomating the testing of a panel can be achieved with optical sensors and feedback to the gamma correction section of the display," it fails to identify any specific structure that performs the function of "executing a predetermined algorithm" using this sensor data. *Id*. at 7:21-23. The specification simply states that once "the optical sensors have modulated gamma reference voltage levels for the columns to achieve the predetermined light matching for the display these values can be saved in the gamma reference circuitry." *Id*. at 7:23-27. In other words, this statement describes only the intended outcome, but fails to disclose what structure, if any, performs the claimed function.

c. Plaintiff's Identified Corresponding Structure Does Not Perform The Function Of The Means For Executing A Predetermined Algorithm…

108. I understand that Plaintiff' has identified a generic programming interface to be the corresponding structure that performs the claimed function. However, Plaintiff's identification is incorrect. While the Plaintiff points to a "programming interface," it fails to specifically identify any "programming interface" described in the specification, such as programming interface 230 shown in Figure 2, or demonstrate how this structure performs the claimed function of "executing a predetermined algorithm according to predetermined criteria and data sensed by said at least one sensor." As I've discussed above in Section IX.C.2.b, the specification establishes that the programming interface serves an entirely different purpose—to facilitate the programming of analog voltage values into analog nonvolatile memory cells. Nothing in the specification discloses that either the programming interface or programming engine executes any algorithm, let alone one that possesses sensor data. The programming interface's function of enabling voltage value programming is fundamentally different from the algorithmic processing function recited in claim

1 of the '788 patent. Plaintiff's identification of this structure therefore fails to satisfy the requirements for a proper means-plus-function analysis under 35 U.S.C. § 112, paragraph 6.

109. Moreover, the specification does not describe a structure that executes a predetermined algorithm based on predetermined criteria and data sensed by a sensor. As discussed above, there is no structure disclosed in the specification that performs the recited function.

110. And notably, the specification only uses the term "predetermined criteria" in the claims of the '788 patent. The specification does not describe what constitutes this "predetermined criteria," what criteria are considered, where the criteria originates, or how it is used by any structure, in combination with sensor data, to allow for execution of a predetermined algorithm. The specification does describe that "[t]he output of a sensor can be matched to a predetermined application condition which selects the corresponding gamma value set." *Id.* at 7:30-32. But the specification provides no guidance to a POSITA about what constitutes a "predetermined application condition" or how that "predetermined application condition" is utilized by any structure that executes a predetermined algorithm.

111. This complete absence of structural disclosure renders the term indefinite under 35 U.S.C. § 112, paragraph 6, as there is simply no guidance in the specification regarding what structure corresponds to the function of "executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor."

3. Gamma Reference Control Capability

"Gamma reference control capability" '788 patent, claim 1	Subject to 35 U.S.C. § 112 ¶ 6 **Function**: At least storing gamma reference voltage levels **Structure**: None (indefinite)

112. I understand that Defendants contend that the term "gamma reference control capability" is a means-plus-function term, but that it is indefinite because there is no corresponding structure to perform the function in the specification.

113. I agree with Defendants. In my opinion, the term "gamma reference control capability" should be construed as a means-plus-function term because the Asserted Claims do not recite a sufficient structure for performing the recited function. The term "gamma reference control capability" is also indefinite because there is not a sufficient structure described in the specification that defines a "gamma reference control capability" and that performs the function of "at least storing gamma reference voltage levels."

a. The Term "Gamma Reference Control Capability" Should Be Construed As A Means-Plus-Function Term

114. In my opinion the term "gamma reference control capability" is a means-plus-function term. As discussed in more detail below, I reach that conclusion on the basis that (1) the term "gamma reference control capability" is not the name of a structure or class of structures known to a POSITA; (2) the full claim language in which phrase "gamma reference control capability" appears does not recite structure for "gamma reference control capability" that is capable of performing the function recited in the claim; and (3) the specification, to the extent that it describes any structure at all, does not define "gamma reference control capability" as those structures.

115. To a POSITA, the term "gamma reference control capability" is not the name of a structure or class of structures known in the art. The term "gamma reference control capability" is not used in the art and is not a term a POSITA would be familiar with. Rather, "gamma reference control capability" appears to be a term coined for the Asserted Patents. To a POSITA, "control capability" is a generic term and "gamma reference" (which a POSITA would understand to be a

gamma reference voltage) is what is being controlled. "Gamma reference control capability" therefore, appears to be a generic stand-in for any structure that can perform the particular controlling-like function for gamma reference voltages.

116. Claim 1 of the '788 patent does not define any structure for the recited "gamma reference control capability," as claim 1 simply states that it can be "electrically reprogrammable and non-volatile." I understand that claim 1 recites that "gamma reference control capability" is "electrically reprogrammable and non-volatile," however, these qualifiers describe functional characteristics rather than any specific structure. To a POSITA "electrically reprogrammable and non-volatile" are simply features, and not a specific structure that performs the claimed function. For example, memory can be electrically reprogrammable and non-volatile but those features do not provide sufficient definition to a POSITA to determine the structure for a "gamma reference control capability."

117. The term "gamma reference control capability" is also not defined in the specification of the Asserted Patents. Specifically, there is no disclosure in the specification where the inventors defined the term "gamma reference control capability" in a lexicographical sense. Nor does the specification suggest that "gamma reference control capability" were known in the art as a particular structure or class of structures. In fact, the term "gamma reference control capability" appears seven times in the '788 patent, recited only in claims 1, 2, 5, and 6 where it is described as "providing said [liquid crystal] display with gamma reference control capability which is electrically reprogrammable and non-volatile," "storing said gamma reference voltage levels in said gamma reference control capability," "wherein the method is repeated more than once under different ambient display conditions to generate at least one different set of gamma reference voltage levels stored in said gamma reference control capability," "retrieving said

gamma reference voltage levels from said gamma reference control capability," and "wherein the calibrating step is repeated more than once under different ambient display conditions to generate at least one different set of gamma reference voltage levels stored in said gamma reference control capability." However, the specification provides no explanation or detail as to what the inventors intended the "gamma reference control capability" to mean.

118. Most notably, the specification does not disclose any specific circuitry, components, architecture, or structural implementation that would constitute the claimed "gamma reference control capability." Because there is a complete absence of disclosure regarding the structure of the "gamma reference control capability," a POSITA would not be able to determine what apparatus or structure performs the function of "at least storing gamma reference voltage levels." This lack of corresponding structure in the specification strongly suggests that the term should be construed as a means-plus-function limitation, even though it does not use the phrase "means for," because the term fails to recite sufficiently definite structure and instead describes a function without providing adequate structural detail for performing that function.

b. The Specification Does Not Identify A Corresponding Structure To Perform The Function Of Gamma Reference Control Capability

119. As discussed above, it is my opinion that the term "gamma reference control capability" is a means-plus-function term. Therefore, I will determine what "function" in the term "gamma reference control capability" performs in the Asserted Claims and what structure(s), if any, is disclosed in the specification that can perform the recited "function."

120. The function of "gamma reference control capability" is recited in asserted claim 1 of the '788 patent. Claim 1 of the '788 patent recites "storing said gamma reference voltage levels in said gamma reference control capability." It follows that the properly understood function of "gamma reference control capability" is at least to "stor[e] [] gamma reference voltage levels." A

POSITA would understand that memory can perform the function of at least "storing gamma reference voltage levels" but the term "gamma reference control capability" would suggest to a POSITA that the structure is not merely limited to memory.

121. As discussed above, the only mention of "gamma reference control capability" in the specification resides in the claims. That is, other than claims 1, 2, 5, and 6, the term "gamma reference control capability" is absent from the entire specification. With respect to asserted claim 1, I mentioned above that it recites that "gamma reference control capability" is "electrically reprogrammable and non-volatile," however, these are only features of what a corresponding structure would include, but not a structure in itself. A POSITA would understand that the features "electrically reprogrammable and non-volatile" are features that can describe a specific type of memory structure, specifically non-volatile memory. But, again, the term "gamma reference control capability" suggests to a POSITA that this "control capability" does more than simply store gamma reference voltage levels.

122. I understand that each embodiment of the '788 patent includes components that have the characteristics of being nonvolatile and/or reprogrammable, however, these characteristics alone are insufficient to inform a POSITA about the specific structure that constitutes the claimed "gamma reference control capability." For example, a POSITA would understand that a "gamma reference control capability" includes non-volatile memory that is electrically reprogrammable but would not understand what other components form the structure of this "control capability." In other words, a POSITA would understand that non-volatile memory is not a "control capability" (it is simply a storage component) but would not understand what components of the structure perform the "control capability." The '788 patent repeatedly describes

functional capabilities without adequately defining the corresponding structure that performs these functions.

123. For instance, the embodiment of Figure 2 describes a gamma reference circuit that includes a programming interface that has a common Analog Input terminal "used to set the reference voltage." *Id*. at 2:62-3:9. As previously stated, "[o]nce a desired voltage is found by varying the Analog Input for a particular channel . . .the value on the Analog Input is written into the nonvolatile memory for the output channel selected." *Id*. at 3:25-28. While this passage indicates that nonvolatile memory is used, it fails to define what constitutes the overall "gamma reference control capability." A POSITA would recognize that nonvolatile memory alone is only a storage device, not a device with "control capability" as claimed. The '788 patent leaves unanswered what additional components or circuitry are required to transform nonvolatile memory into the claimed "gamma reference control capability."

124. Figure 3, which discloses the gamma reference controller of Figure 2, also references a memory device in the form of "programmable analog floating gate memory cells" where the '788 patent states that the "mux 320 connects signals from the programming engine 310 to any one of the programmable analog floating gate memory cells." *Id*. at 3:56-4:1. While this description identifies individual components (mux, programming engine, and programmable analog floating gate memory cells), the '788 patent fails to explain which, if any, alone or in combination, represents the claimed "gamma reference control capability." The '788 patent only identifies certain components without clarifying their structural relationships, thereby leaving a POSITA blind about what exactly comprises the claimed "control capability."

125. The AG1818 of Figure 6 includes a programming interface which allows the AG1818 to be programmed. *Id* at 6:22-23. Further, the AG1818's programming interface consists

of four signals, including V_{PP}, "a high voltage input [that] . . . provides high voltage pulses to program individual cells," these individual cells being "analog nonvolatile storage cell[s]." *Id*. at 5:40-41, 6:27-30. Here too, while the '788 patent identifies certain components, they again fail to define the bounds of what constitutes the claimed "gamma reference control capability." A POSITA would find it difficult to ascertain whether this "capability" encompasses aside from the memory cells themselves, such as if it necessarily includes the programming interface, or additional elements like the "bank switching capability" mentioned elsewhere in the '788 patent. *Id*. at 7:9-10.

126. To a POSITA, the structure of a "gamma reference control capability" would not be limited to non-volatile memory that is electrically reprogrammable. Instead, the term "capability" itself implies more than simply storing values, it suggests an ability to perform a function of controlling gamma reference voltage values that would not be performed if voltage values are simply stored. However, the '788 patent is silent as to what delineates a specific structure which provides this "capability."

127. A POSITA, after reading the '788 patent, would be left uncertain about whether the "gamma reference control capability" refers solely to memory elements, or whether it necessarily includes additional components such as programming engines, interfaces, multiplexers, or other elements mentioned throughout the specification. This ambiguity renders the term indefinite, as it fails to provide the "corresponding structure, material, or acts" required for means-plus-function claiming under 35 U.S.C. § 112, paragraph 6.

128. Moreover, during the prosecution of the '788 patent, the Examiner rejected claim 1 as obvious over U.S. Patent No. 6,593,934 ("Liaw"). Here, the Examiner had stated that Liaw disclosed "providing said display with gamma reference control capability" in the form of Liaw's

automatic gamma parameter correction system disclosed in Figures 7A-B of Liaw[2]. Phenix_AUO_Hisense_0000504-505 (Examiner's Non-Final Rejection). Figure 7A of Liaw, reproduced below, includes numerous components such as a display, main controller, back-lighting control unit, adjusting means, programmable gamma voltages generating means, switch control unit, programmable switch(es), voltage dividing circuit, and output buffers.

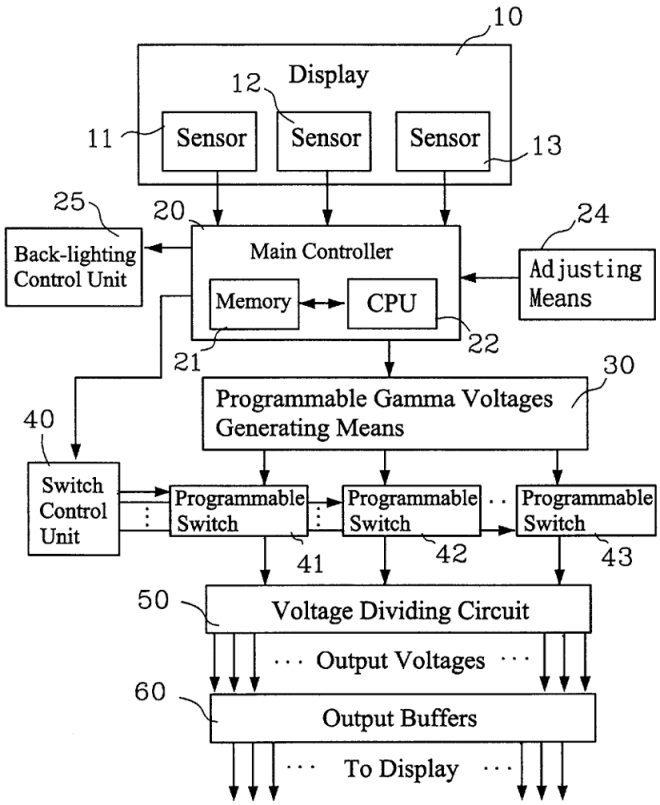


FIG. 7A

129. In responding to this rejection, the Applicant notably did not challenge the Examiner's characterization of Liaw's "automatic gamma parameter correction system" as the

[2] The Examiner also cited to Liaw at 5:62-6:2 in support of their opinion that Liaw discloses the recited "gamma reference control capability." '788 FH at __. This portion of Liaw's specification does not use the term "gamma reference control capability" or otherwise provide a POSITA any indication about what structure from Liaw Figures 7A and 7B would be included in a "gamma reference control capability." A POSITA would not understand that a "gamma reference control capability" would include every component from Liaw's Figures 7A or 7B because, for example, both figures include a display. But claim 1 of the '788 patent recites that the method "provid[es] said display with gamma reference control capability" suggesting to a POSITA that a "gamma reference control capability" does not include a display.

claimed "gamma reference control capability." Nor did the Applicant identify what components would or would not be included in Liaw's "gamma reference control capability." Instead, the Applicant agreed that the cited portion of Liaw discussed Liaw's "automatic Gamma parameter system" but disagreed that such "automatic Gamma parameter system" is a "control capability" that is non-volatile or electrically reprogrammable. Phenix_AUO_Hisense_0000485 (Applicant's Response to Examiner's Non-Final Rejection) (arguing "[t]he cited reference also does not disclose providing gamma reference control capability 'which is electrically reprogrammable and nonvolatile'"). A POSITA, therefore, would understand that some portion discloses a "gamma reference control capability" but would not understand what components comprise the structure of this "control capability" or what components do not.

130. Applicant's failure to challenge the Examiner's interpretation of "gamma reference control capability" indicates to a POSITA that the term itself does not denote a specific, well-understood structure in the art. In my opinion, this exchange during prosecution reinforces that "gamma reference control capability" is indefinite, lacking any definite structural meaning in the art.

131. The '788 patent's inability to define a structure of the recited "gamma reference control capability" renders the term indefinite under 35 U.S.C. § 112, paragraph 6, as there is simply no guidance in the specification regarding what structure programs "control capability" to gamma reference voltage values. A POSITA would understand that non-volatile memory that is electrically reprogrammable must be part of the structure but would not understand what other components are included in the structure of a "gamma reference control capability," and specifically what components would provide the "control capability."

4. Predetermined Algorithm

"Predetermined Algorithm" '788 patent, claim 1	Indefinite

132. In my opinion, the proper construction for "predetermined algorithm" in view of the specification, is that it is indefinite. Claim 1 of the '788 patent recites, in part that a "predetermined algorithm" optimizes gamma reference voltage levels based on "predetermined criteria" and data sensed by the at least one sensor. I understand that when the term "algorithm" is disclosed in a claim, the specification must disclose said algorithm. Based on my review of the specification, however, the '788 patent fails to disclose any specific algorithm for optimizing gamma reference voltage levels based on predetermined criteria and sensor data, rendering the claim indefinite under 35 U.S.C. § 112, paragraph 6.

133. As an initial observation, the terms "predetermined algorithm" and "predetermined criteria" do not appear in the body of the specification. Instead, these terms are only recited in claims 1, 3, and 5 of the '788 patent. Moreover, any mention of "optimizing," "optimization," or "optimization algorithms" occurs three times in the body of the specification, and none of these limited references disclose an actual "predetermined algorithm" that is required by claim 1. For example, the specification states that a "PC based programming interface is available for prototyping and gamma optimization," and that "[d]isplay optimization algorithms may be located in such a PC which also may be connected to monitors feeding back data from the display during the optimization tuning at time of manufacture." *Id*. at 7:13-19. However, this disclosure does not provide any specific algorithm for optimizing gamma reference voltage levels based on predetermined criteria and sensor data.

134. A POSITA would know what an "algorithm" is but, similar to the term "control circuit" discussed above, without additional details or context about the "algorithm," a POSITA would be unable to determine the particular steps and order of execution of these steps for the "algorithm." The addition of "predetermined" as a descriptive term for the "algorithm" is unhelpful. There is no explanation or context of what is "predetermined" or the criteria that the "predetermined algorithm" is based on.

135. As discussed previously, Figure 2 describes a gamma reference circuit implementation which utilizes gamma reference controllers for a TFT panel as well as a "Programming Interface 230 [which] comprises a common Analog Input (A_{IN}) used to set the reference voltage." *Id*. at 2:62-3:9. According to the specification, the programming engine 230 operates in two distinct modes: a normal mode where " the R/W pin is pulled High and the reference voltage outputs will reflect the value last programmed into the nonvolatile memory cells" and a writing/programming mode where "the device enters Tracking Mode" whereby "the output of the selected channel tracks the input voltage on the Analog Input" and "[o]nce the desired voltage is found by varying the Analog Input for a particular channel, the R/W signal is driven high and the value on the Analog Input is written into the nonvolatile memory." *Id*. at 3:14-29.

136. This description of Figure 2's programming interface 230 depicts an adjustment process to "vary" inputs until a "desired voltage is found," and not an automated process executing a "predetermined algorithm" that optimizes gamma reference voltage levels based on "predetermined criteria" and sensor data as required by claim 1 of the '788 patent. Neither Figure 2 nor its accompanying description discloses any algorithm, much less one capable of automatically optimizing voltage levels using sensor data based on predetermined criteria. Instead, the '788 patent only describes a tuning process.

137. The embodiment in Figure 3, disclosing an embodiment of the gamma reference controllers shown in Figure 2, includes a programming engine 310 with an Analog Input terminal "used to set [a] reference voltage level." *Id*. at 3:52-55. Like the embodiment in Figure 2, the gamma reference controller has a "read mode" where "all channels continuously output their corresponding stored voltages" and a "track and write cycle" mode where the addressed channels outputs "a voltage equal to the voltage applied to the Vin pin, multiplied by [a] voltage multiplication factor M." *Id*. at 4:21-26.

138. This description of Figure 3's programming engine adjustment process used to store an analog voltage value is not based on any optimization process using sensor data or predetermined criteria. Nor does Figure 3's programming engine adjustment process describe execution of any predetermined algorithm. Instead, the specification describes a programming mechanism to write analog voltage values into programmable analog floating gate memory cells. Moreover, it does not disclose any algorithm that determines the optimal analog voltage values based on sensor feedback. The ability to store analog voltage values in programmable analog floating gate memory cells does not constitute the disclosure of a specific "predetermined algorithm" as required by claim 1 of the '788 patent.

139. The embodiment in Figure 6, disclosing the AG1818, a programmable gamma reference generator with integrated output buffers, also fails to disclose a "predetermined algorithm" that optimizes gamma reference voltage levels based on "predetermined criteria" and sensor data. Rather, the AG1818's programming interface allows for a device to be "programmed in-situ . . . or [to] adjust the gamma reference voltages of an individual display." *Id*. at 6:22-25. The programming interface of the AG1818 includes four signals, including V_{PP}, a "high voltage

input used to select the programming mode and also provides high voltage pulses used to program individual cells." *Id*. at 6:27-30.

140. In my opinion, the AG1818 fails to disclose a "predetermined algorithm" that optimizes gamma reference voltage levels based on "predetermined criteria" and data sensed by the at least one sensor. Instead, what's described here is a process for programming and storing analog voltage values that have already been determined through unspecified means. The specification explains how to address memory locations, how to enter programming mode, and how to write values to memory cells, but is silent on how those analog voltage values are systematically determined in the first place. There is also an absence of any disclosed process for utilizing sensor data with optimized analog voltage values based on predetermined criteria to execute an algorithm that achieves a desired gamma curve.

141. The specification further discloses an alternative method for programming the individual analog nonvolatile cells. The process involves placing the AG1818 into the "Program Mode" where a particular bank is addressed through a designated sequence of address inputs, followed by applying a pulse to the V_{PP} pin in order to latch the bank address. *Id*. at 6:37-42. Subsequently, the specific "cell to be programmed in the selected bank is addressed" through another sequence of inputs, followed by pulsing V_{PP} again. *Id*. at 6:42-44. "Programming of the selected storage cell" occurs by "pulsing V_{PP} with adjustable voltage pulses between approximately 8 and 14 volts." *Id*. at 6:45-47. When the cell reaches "the desired voltage level," the device is returned to read mode through another specific sequence of address inputs and V_{PP} pulsing. *Id*. at 6:47-50.

142. Even this alternative process of programming the AG1818 fails to disclose a "predetermined algorithm" that optimizes gamma reference voltage levels to achieve a desired

gamma curve based on "predetermined criteria" and data sensed by the at least one sensor. Rather, the specification describes a procedure for writing analog voltage values to analog nonvolatile cells. The programming sequence explains how to store analog voltage values, not how to systematically determine what those optimal values should be based on sensor data and predetermined criteria. The process focuses on memory addressing and writing. That is, setting address lines, pulsing voltage pins, latching addresses, and applying programming pulses. There is not a disclosure of how the "desired voltage level" or "desired gamma curve" is determined through any optimization process. In addition, the process is silent on any sensor data input, any predetermined optimization criteria, or any systematic method for processing such inputs to determine optimal analog voltage values.

5. Gamma Reference Voltage Levels

"Gamma Reference Voltage Levels" '788 patent, claim 1	an analog voltage(s) stored in an analog storage cell

143. In my opinion, the proper construction for "gamma reference voltage levels" in view of the specification is "an analog voltage(s) stored in an analog storage cell." While the term "gamma reference voltage levels" would be a term that a POSITA is familiar with, a POSITA would look to the specification of the '788 patent to determine whether the recited "gamma reference voltage levels" are limited to an analog voltage value, or whether they can include a digital representation of the gamma reference voltage level. Based on the specification of the '788 patent, a POSITA would conclude that the term "gamma reference voltage levels" is described as, and therefore intended to be an analog voltage value that represents the gamma reference voltage level, and would not include a digital representation, as one is not identified.

144. Figure 2 describes an architectural diagram illustrating a gamma reference circuit implementation employing "gamma reference controllers, 210 and 220 [light green], for a TFT panel 280 [purple]," where the gamma controller 210 "drives a first set of eight gamma reference voltages GM1-GM8 to the sources drivers [pink]" and the gamma reference controller 220 "drives a second set of eight gamma reference voltages GM9-GM16 to the source drivers." '305 patent at 2:62-3:6.

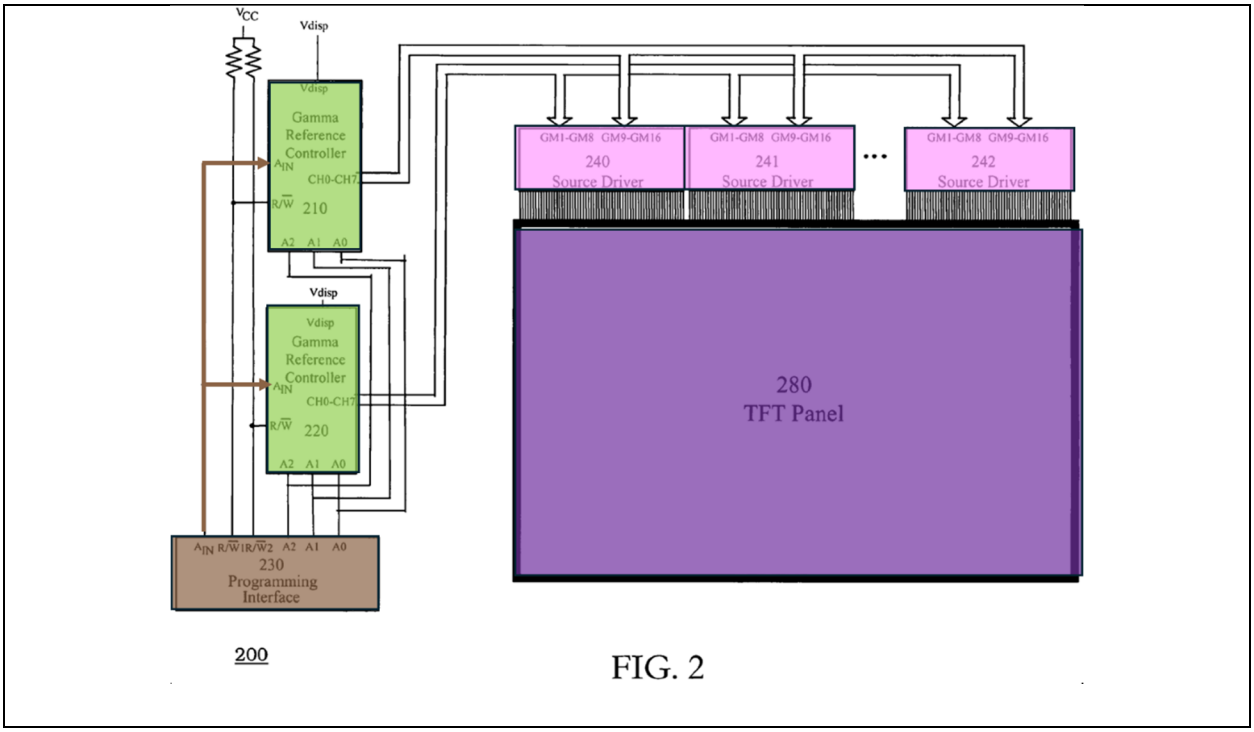


FIG. 2

145. According to the specification, the programming interface 230 (brown) includes an Analog Input ("A_{IN}") terminal which is used to "set the reference voltage level" while the address inputs A_0 through A_2 determine "which reference level is being written." *Id.* at 3:7-10. Further, the specification describes distinct operational modes that appear to inherently rely on analog signal processing. For instance, during "normal operation," the R/W terminal on the programming interface 230 is "pulled High and the reference voltage outputs will reflect the last value programmed into the nonvolatile memory cells." *Id.* at 3:14-16. During a "writing or programming operation," the device selects a specific output channel using address inputs A_2-A_0, the R/W pin is

pulled low, and the device enters "Tracking Mode" where "the output of the selected channel tracks the input voltage on the Analog Input," with the specification explicitly noting that an internal voltage multiplier may convert the 0 through 3 volt Analog Input to a 0 through 10 volt output range. *Id*. at 3:17-24.

146. A POSITA would understand this direct voltage tracking and conversion process demonstrates that the gamma reference voltage generation system operates using analog signals throughout the signal path. Additionally, the specification explicitly mentions that the "traditional approach to the Gamma Reference Generation problem has been to use Select-On-Test Resistors," as these resistors, while the "least expensive solution" to this problem, allow for "reference voltages to be fine-tuned to the requirements of the individual display." *Id*. at 1:28-41. Moreover, the specification appears to teach away from a digital approach as "digitally-controlled potentiometers (DCPs) and Digital to Analog Converters (DACs)" because while they could better perform the functions associated with Select-On-Test resistors, their associated costs were unacceptable. *Id*. at 1:39-45; *see also id.* at 2:4-12 (rejecting the inventions described in U.S. Patent Nos. 6,593,934 and 6,046,719 because "[b]oth inventions teach quite complex digital approaches to this 'analog problem'; consequently both inventions are quite expensive" and that it is instead desirable to design a gamma reference architecture that "provides reprogrammable capability and achieves acceptable cost").

147. In addition, Figure 3 of the specification depicts the gamma reference controller from Figure 2. Here, the Analog Input from the programming interface 230 from Figure 2 directly feeds into an Analog Input terminal of both gamma reference controllers 210 and 220 of Figure 2 (brown arrow).

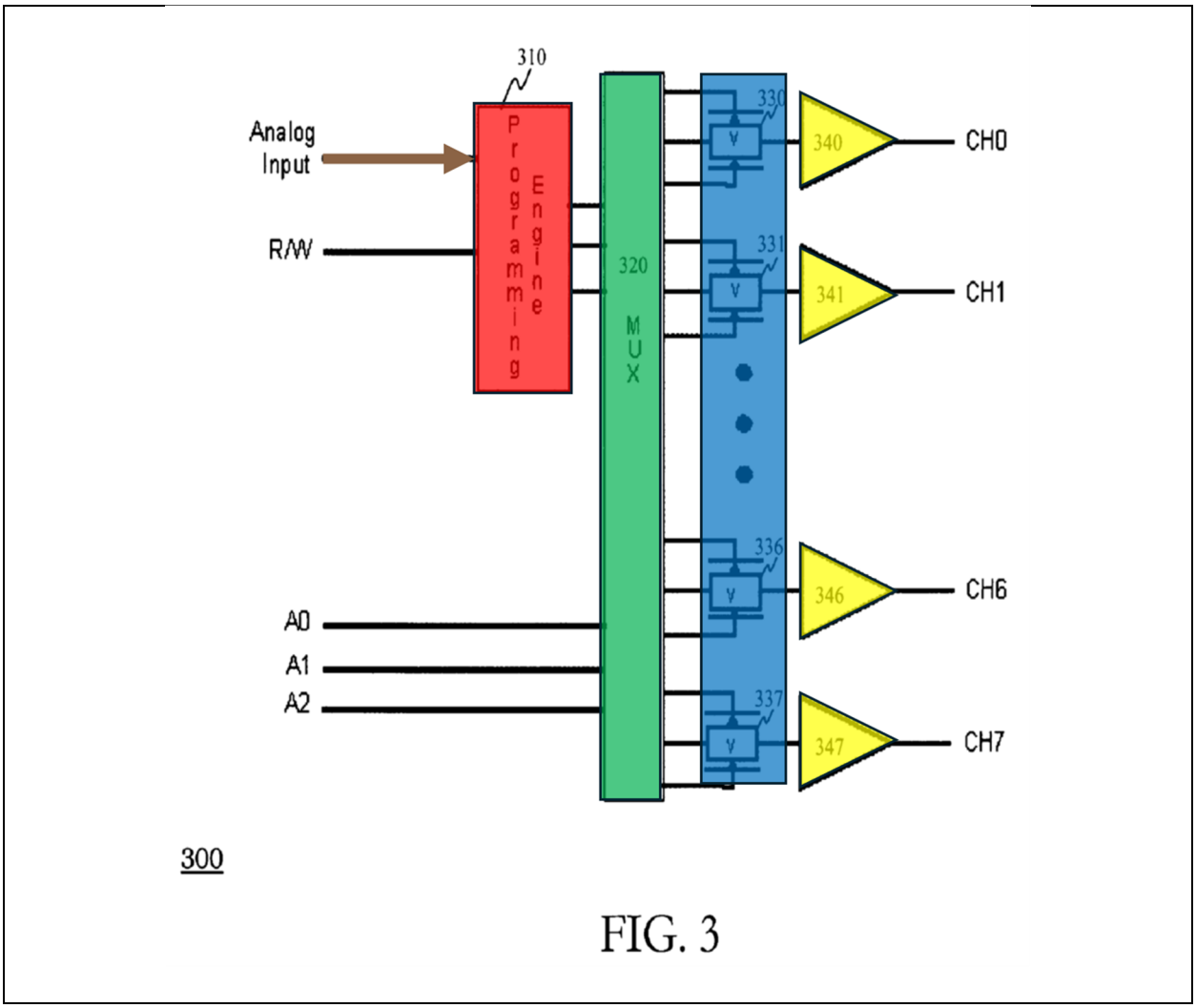


FIG. 3

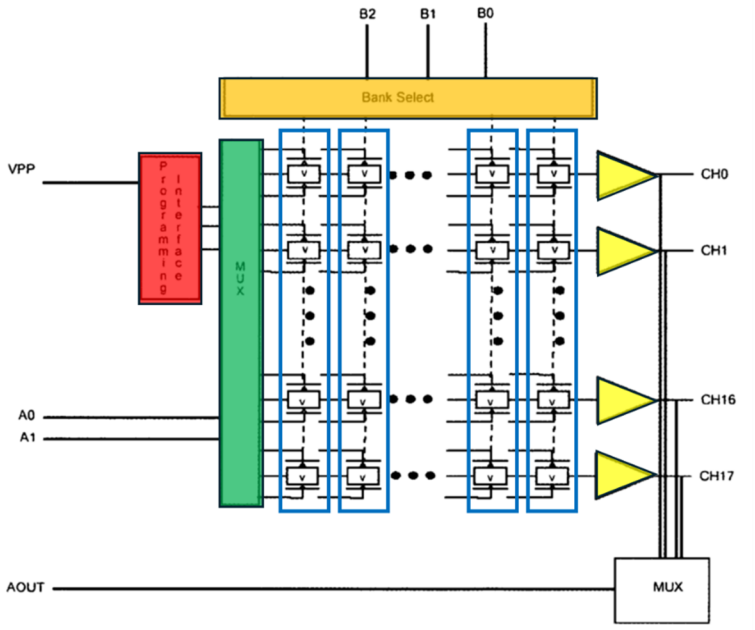
148. The gamma reference controller of Figure 3 includes a "programming engine or interface 310 [red], a mux 320 [green], programmable analog floating gate memory cells 330, through 337 [blue], and drivers 340 through 347 [yellow]." *Id.* at 3:48-52. Like Figure 2, the programming engine 310 has an Analog Input terminal which is used to "set the reference voltage level . . . for a corresponding gamma reference controller." *Id.* at 3:52-56. The mux 320, which is positioned in between the programming engine 310 and a column array of programmable analog floating gate memory cells 330 through 337, allows for signals from the programming engine 310 to flow to any one of the aforementioned analog floating gate memory cells. *Id.* at 3:56-4:2.

149. Based on my review of the specification and Figure 3, each output channel (CH0 through CH7) connects directly to an analog storage cell designed to store analog values with 1024-step (10-bit) resolution. *Id*. at 4:4-6. Additionally, I understand this to mean that the '788 patent contemplates storing actual analog values, not digital representations that would later require conversion, via a digital to analog converter, which the patent explicitly mentions would not be cost effective. *Id*. at 1: 41-45("Devices such as . . . digitally-controlled potentiometers (DCPs) and Digital to Analog Converters (DACs) all could perform this function in some ways better than the Select-On-Test resistors, but the cost is unacceptable."). Moreover, the gamma reference controller of Figure 3 also discloses the presence of an internal voltage multiplier with a multiplication factor of M, capable of producing output voltages ranging from 0 to approximately 13.5 volts or alternatively 16 volts. *Id*. at 4: 9-11.

150. Like the embodiment of Figure 3, Figure 6, depicting the AG1818 integrated circuit, also generates analog gamma reference voltages. The AG1818 has eighteen output channels providing "an output range of 0 to 13.5 Volts," where each output is also "internally connected to an analog nonvolatile storage cell which can be written with 1,024 analog values . . . to better than 15 mV resolution." *Id*. at 5:38-43. The AG1818 includes a "programming interface [red] [that] allows the device to be programmed." *Id*. at 6:22-23. The programming interface includes a V_{PP} terminal used to not only select a programming mode, but also to provide "high voltage pulses used to program the individual" analog nonvolatile storage cells. *Id*. at 6:27-30.

FIG. 6

BLOCK DIAGRAM (AG1818)



151. Based on my understanding of the specification, it is evident that the AG1818 operates as an analog device. For instance, programming of the selected analog nonvolatile storage cell is initiated by "pulsing V_{PP} with adjustable voltage pulses between approximately 8 and 14 volts." *Id*. at 6:45-47. The specification further denotes that "[k]ey variables in the programming process are programming voltage amplitude, rise and fall time of the pulse, and pulse duration"—all analog characteristics. *Id*. at 6:54-56. In addition, and perhaps most telling, the specification emphasizes that real time monitoring of the analog nonvolatile storage cell "voltage level is accomplished through the A_{OUT} pin which reflects the [analog nonvolatile storage] cell voltage at its output buffer which is the voltage that is applied to the display column." *Id*. at 6:58-61.

152. In other words, the entire signal path maintains analog integrity throughout—from the initial programming interface receiving analog voltage pulses, to the storage of precise analog values in nonvolatile memory cells, to the direct application of these voltages to display columns

without any digital-to-analog conversion. A POSITA, having reviewed the '788 patent would have understood that this uninterrupted analog signal processing architecture confirms that the gamma reference voltage generator was designed as an inherent analog solution.

153. Moreover, nothing in the specification would suggest to a POSITA that the inventors contemplated implementing the gamma reference voltage generator as a digital signal requiring conversion to an analog form. Rather, the specification consistently describes an analog signal path from programming through storage and ultimately to output, confirming that the claimed "gamma reference voltage levels" were conceived, disclosed, and intended to function exclusively as analog signals.

154. Lastly, the extrinsic evidence also supports that "gamma reference voltage levels" should be construed as "gamma voltage values saved in a gamma reference circuitry, configured to be set by an analog input and applied, as an analog output, to columns of a panel of a display, the voltage values being modulated by optical sensors to achieve a predetermined light matching for the display." The IEEE Dictionary defines "voltage level" in data transmission systems as "the ratio of the voltage existing at that point to an arbitrary value of voltage used as a reference," in systems such as televisions "where wave shapes are not sinusoidal or symmetrical about a zero axis and where . . . the voltage level is the ratio of the peak-to-peak voltage existing at any point in the transmission system to an arbitrary peak-to-peak voltage used as a reference." Similarly, the term "reference voltage" in analog computing contexts is defined as a "voltage used as a standard reference, usually the nominal full scale of the computer."

155. My understanding of these definitions in conjunction with the specification clearly indicates to me that "gamma reference voltage levels" operate in the analog domain, involving voltage ratios and continuous values, and not digital representations. Applied to the context of

the '788 patent, a POSITA would understand that "gamma reference voltage levels" must be analog gamma voltage values configured to be set by an analog input and applied as an analog output to columns of a display panel. This understanding aligns with the patent's description of a system where voltage values are directly modulated to achieve predetermined light matching for displays, without any suggestion of digital-to-analog conversion in the process.

6. Non-Volatile Storage Cells

"Non-volatile storage cells" '305 patent, claims 1-2	Analog memory cells which retain stored data even when power is removed

156. In my opinion, the proper construction for "non-volatile storage cells" in view of the specification is "analog memory cells which retain stored data even when power is removed." While I understand that the term "non-volatile storage cells" was construed by the Court in the *Wistron* Litigation to mean "memory cells which retain stored data even when power is removed," I disagree with the Court's construction because it is not limited to analog memory cells. As discussed below, a POSITA would understand that the '305 patent is limited to an analog solution and teaches away from using a digital solution, such that the "non-volatile storage cells" recited in claim 1 of the '305 patent is limited to analog non-volatile storage cells.

157. As an initial matter, and as discussed throughout this Declaration, the specification of the Asserted Patents expressly recognizes the shortcomings of traditional gamma reference generation using Select-On-Test resistors. While the specification acknowledges that alternatives such as digitally-controlled potentiometers (DCPs) and digital-to-analog converters (DACs) can, in some respects, outperform Select-On-Test resistors, it makes clear that their associated costs are unacceptable. *Id*. at 1:39-45. The specification further describes prior inventions which eliminated select-on-resistors employing "digital approaches to this 'analog' problem," however, the

"inventions [were] quite expensive." *Id*. at 2:4-9. Instead of looking to a costly digital solution, the specification stresses that "it is desirable to design a gamma reference architecture that automates gamma adjustment and provides reprogrammable capability and achieves an acceptable cost." *Id.* at 2:10-12.

158. Also discussed throughout this Declaration, the specification of the Asserted Patents discloses embodiments utilizing non-volatile storage cells, where each time these cells are described only as analog memory cells. The Asserted Patents consistently characterize these cells as storing analog voltage values rather than digital binary data, and describe their function in maintaining gamma correction values after power cycling.

159. For example, the programming interface 230 of Figure 2 provides an Analog Input (A_{IN}) specifically designed to "set the reference voltage level," which is directly "written into the nonvolatile memory" when the desired voltage value is achieved through "varying the Analog Input for a particular channel," confirming that these cells store analog voltage values rather than digital data. *Id*. at 3:7-29. In addition, the embodiment illustrated in Figure 3 explicitly mentions that the "programming engine 310, coupled to the mux, comprises an Analog Input which will be used to set the reference voltage level" and a "mux 320 connects signals from the programming engine 310 to any one of the programmable analog floating gate memory cells" with each output being "internally connected to an analog storage cell which can be written with analog values." *Id*. at 3:49-4:5. Table 1, depicting an alternative pin description for the gamma reference controller reinforces the fact that V_{IN}, designating the Analog Input, is an analog input voltage ranging from 0 volts to 3 volts and that "the voltage on the analog input [is written] into the appropriate analog memory location." *Id*. at Table 1 (annotated).

TABLE 1

Name	Description	Value Range	Function
VDD	Supply Input	3 V to 5.5 V	
Vdisp	Display Supply	10 V to 12 V	
R/W	Read/Write	CMOS Input	When driven to an active low input, places the selected output into tracking mode. The Rising Edge of R/W writes the voltage on the analog input into the appropriate analog memory location
Rdy	Device Ready	TTL Compatible Output	
VSS	Ground		
CH0–CH7	Analog Outputs	0 V–10 V	Analog Output Voltage Channels
VIN	Analog Input	0 V–3 V	Analog Input Voltage
A0–A3	Address Inputs	CMOS Inputs	Selects which output is placed in tracking mode or is written to during a write operation

160. Even the AG1818 embodiment of Figure 6 has each output channel being "internally connected to an analog nonvolatile storage cell which can be written with 1,024 analog values, providing . . . better than 15 mV resolution." *Id*. at 5:38-43. Figure 4A, which provides an alternative pin description for the AG1818 also emphasizes that the V_{PP} pin provides the "programming voltage . . . to program the analog memory cells." *Id*. at Figure 4A (annotated).

FIG. 4A

PIN DESCRIPTIONS

Name	Description	Value Range	Function
VDD	Digital Supply Input	3V to 3.3V	
CH0-CH17	Analog Outputs	0V –VREF-0.2	Analog Output Voltage Channels
B0-B2	Bank Select	CMOS Inputs	Selects which output is placed in tracking mode or is written to during a write operation
VREFH	Output High Level Reference	5-13.5 Volts	Sets the highest voltage for the output channels.
A_{OUT}	Analog Output	0.2V-VREFH-0.2	Outputs the current value of the selected channel of the selected bank during programming
V_{PP}	Programming Voltage	10-14Volts	Provides the programming voltage and timings needed to program the analog memory cells. Also used to enter operating modes other than read.
A0-A1	Address Inputs	TTL	Used to Select Programming Modes and Locations to be written

161. In fact, each embodiment discussed in the '305 patent (and consequently the '788 patent) shows non-volatile storage cells to be exclusively analog memory cells storing analog values or voltages, with no mention or suggestion of digital alternatives. A POSITA would not only understand that the specification teaches non-volatile storage cells to be analog in nature, but also that the specification teaches away from digital solutions evidenced by the criticism levied against the use of costly DACs.

162. The extrinsic evidence also supports the construction that non-volatile storage cells should be construed as "analog memory cells which retain stored data even when power is removed" or "memory cells storing analog voltages, which retain the stored voltages even when power is removed." For example, both the IEEE Technical Dictionary and the McGraw-Hill Dictionary define nonvolatile storage as a "type of storage whose contents are not lost when power is lost" and "a computer storage medium that retains information in the absence of power, such as a magnetic tape, drum, or core." The IEEE Technical Dictionary further describes the term

"Analog" to mean "[p]ertaining to representation by means of continuously variable physical quantity . . . describe[ing] a physical quantity, such as voltage."

163. My understanding of these definitions in conjunction with the specification clearly indicates to me that "non-volatile storage cells" store analog voltage values, and not digital data. A POSITA would also understand that "non-volatile storage cells," as applied to the context of the Asserted Patents, must be analog memory cells that store analog voltage values as the IEEE definition explicitly characterizes analog representation as involving "continuously variable physical quantities" like a voltage.

164. Lastly, I understand that this term was previously construed in the *Wistron* Litigation, and the Court had rejected limiting "non-volatile storage cells" to an analog-only interpretation. After thorough examination of the specification, I respectfully disagree with the previous Court's construction. The specification consistently and exclusively describes these cells as analog storage elements with specific analog voltage values and resolution. The Asserted Patents' detailed programming methodology—involving incremental voltage adjustments, real-time monitoring, and closed-loop verification—is, in my opinion, incompatible with digital storage and only functions with true analog memory cells. Based on this comprehensive and consistent characterization throughout the specification, a POSITA would understand this term to be limited to analog non-volatile storage cells that maintain precise voltage values even when power is removed.

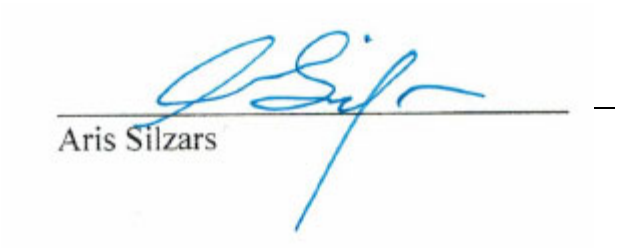
X. CONCLUDING REMARKS

165. This declaration is based on information currently available to me. I reserve the right to supplement and/or modify this declaration to address any information obtained, or positions taken, as this matter continues.

166. I anticipate in my trial testimony, if needed, using some of the above referenced documents and items, or other information and materials that may be provided during the course of this proceeding (such as deposition testimony), as well as representative charts, graphs, or diagrams that will be based on those documents, items, information, and materials to support, summarize, and explain my testimony at trial.

167. I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct to the best of my knowledge and understanding.

Executed on May 7, 2025.



Aris Silzars

APPENDIX 1

ARIS K. SILZARS
19916 NE 30th Court • Sammamish, WA 98074
Phone 425-898-9117, e-mail silzars@attglobal.net

QUALIFICATIONS SUMMARY

Over thirty -years of increasingly responsible technology, marketing, general management, and business development experience in meeting customer needs with high-performance electronic products.

* Extensive experience in positioning technology-based products for competitive advantage, including the identification of distinctive competencies and market differentiating factors.
* Proficient at creating new products and new opportunities through understanding of technology, manufacturing, and the assessment of business and market opportunities.
* A skilled manager of complex multi-technology product developments requiring invention and new technology introduction.
* Well-known internationally as an expert on display technologies through presentations, publications, and technical society leadership.

PROFESSIONAL EXPERIENCE

1995 - Present **NORTHLIGHT DISPLAYS - SAMMAMISH, WA.**

Founder and President

Business development, technology support, and strategic consulting for established and emerging Information Display companies.

* Relocated to the Northwest and founded a new business providing technology development, technology forecasting, and applications support to Information Display businesses and new ventures.
* Created an industry forum for Display Technologies and Display Manufacturers by founding the DisplayWorks industry conference as a joint venture sponsored by SID, SEMI, and USDC.
* Developed the concept of a "virtual" corporation serving the display community with an international support base including partnering relationships with technologists in Russia, France, Japan, Korea, and Princeton and San Jose in the US.
* Positioned the company to become an international resource center for Information Display technology developments and applications.

1994 - 1995 **SARNOFF CORPORATION - PRINCETON, NJ.**

Director of the Display Research Laboratory

Technology leadership, development, and marketing for all display technologies -- CRTs, FEDs, Plasma, LCDs, EL, and Phosphors.

* Increased the laboratories contract revenue by more than $5 million in less than one year.
* Developed a new business strategy and repositioned the group to become the

principal display representatives of the Sarnoff Corporation to government and industry.

* Created a "Center of Excellence" for Field-Emission Technology by bringing in key new contracts and by working with government and industry partners.

1993 - 1994 **DUPONT CO. - Advanced Composite Materials - NEWARK, DE.**

Senior Consultant for Electronics

Business development of new materials technologies for applications in electronics.

* At the request of DuPont management, assessed the electronics business potential and technology competitiveness of: Metal-Matrix Composites, Aramids, Pitch-Carbon Fibers, Metallized Kevlar, Diamond Films and Fibers, Photopolymers, and High-Temperature Superconducting Materials.

* Applied new-technology marketing experience to provide business plans for coated fibers as electron-emitters for flat-panel displays and Thermount® (Kevlar/Nomex Aramid) as a substrate material for Multi-Chip Modules.

* Developed new patentable concepts for products using metallized Kevlar, display structures incorporating coated fibers, holographic filters for color displays, and a low-cost manufacturing process for Metal-Matrix Composites.

1990 - 1993 **LANXIDE ELECTRONIC COMPONENTS, L.P., NEWARK, DE.**

President and CEO

Strategic planning, business development, and operations responsibility for the start-up of an electronics business based on composite materials technology developed by the parent Lanxide Corporation.

* Developed the business plan, adapted the materials technology, established a salable product base, and achieved the first $5MM+ of orders to military and commercial customers.

* Worked with DuPont, the funding partner, to scale-up the technology to achieve volume manufacturing capability at competitive cost.

* Implemented a team oriented company culture and trained 50+ employees in the skills of new business development, manufacturing scale-up, MRP II, and TQM.

1988 - 1990 **INTERCHIP SOLUTIONS, INC., BEAVERTON, OR.**

President/CEO and Founder

Business development and marketing responsibility for the start-up of a Multi-Chip Module Company.

* Developed the Business Plan, assembled a management team, and worked with a variety of investors to successfully achieve first-round financing.

* Determined and prioritized the needs of system designers (the customers), positioned the company to effectively respond to those needs, and accomplished the first sale of products.

* Implemented partnerships with companies supplying CAE tools, fabrication technology, and test equipment.

1974 - 1988 **TEKTRONIX, INC., BEAVERTON, OR.**

(1984 - 1988) General Manager, Hybrid Components Operation

Managed the transformation of this 500 employee 125,000 sq. ft. facility from an internal service organization to an independent business unit with sales to Tek divisions and outside customers.

* Developed the marketing and sales strategy that resulted in $10MM+ of new external hybrids business in less than 2 years.
* Increased sales to internal Tektronix customers from $30MM to $38MM during a period of no growth in the company.
* Improved the division's financial performance from an $8MM/year loss to profitability.
* Established and managed a sales organization, independent from Tektronix Corporate sales, to serve the hybrid and IC businesses.
* Identified new business opportunities and expanded the Hybrid and Ceramics product lines with the introduction of multi-layer ceramic packages and electro-optic components.
* Improved product delivery and quality, reduced inventories, and eliminated shortages through organization-wide use of MRP II and Just-in-Time principles.

(1980 - 1984) Director, Solid State Group

Provided the strategic leadership and management for the development, product application, and manufacturing of all semiconductor and component integration technologies including, Bipolar IC's, MOS IC's, Hybrids, and Ceramic Components. The facilities were located in two buildings (250,000 sq. ft. total) and employed over 900 people.

* Established the strategy and implementation of CAE tools for the design and layout of ICs and hybrids.
* Successfully managed the design and start-up of a new 50,000 sq. ft. IC facility, the installation of a very high-speed bipolar process, and the introduction of E-beam lithography.
* Developed and initiated the manufacture of analog ASICs (Quick-Chip), CCD arrays, and high-speed signal acquisition devices (Si and GaAs).
* Identified the need and implemented the large scale use of Hybrids and Custom IC's into Tek's next generation portable oscilloscopes, the Company's highest revenue products.

(1974 - 1980) Manager, Component Development Group

Increasing responsibility for the selection, development, and implementation of new component technologies into Tektronix products. Managed the company's R&D activities in displays, hybrid circuits, monolithic IC's and electro-mechanical components with a staff of 350 engineers and technicians.

* Guided the technology selection and development of high-performance CRTs, micro-channel plate CRT's, and signal processing devices.
* Initiated the development of GaAs technology at Tektronix, which later resulted in the formation of TriQuint Semiconductor.

1969 - 1974 **WATKINS-JOHNSON CO., PALO ALTO, CA.**

Section Head - Program Manager - Senior Engineer

Developed and promoted Electron Beam Semiconductor devices for military signal processing applications including broadband microwave amplifiers, high-power bandpass RF amplifiers, and high current nanosecond risetime modulators.

EDUCATION

Ph.D., E.E. - University of Utah, 1969
M.A., Physics - University of Utah, 1965
B.A., Physics - Reed College, Portland, OR., 1963

MEMBERSHIPS & PROFESSIONAL ACTIVITIES

Society for Information Display – Convention and Bylaws Committees Chair.
Past President and Past Member of the Executive Committee.
Past Senior Member of the IEEE.
General Chair of the 2005 and 2006 SID Business Conference.
General Chair of the 2004 Society for Information Display Symposium.
General Chair of the 1985 Custom Integrated Circuits Conference.
General Chair of the 1987 Society for Information Display Symposium.
Organizer and Chair of the First Display Manufacturing Technology Conference San Francisco, January 1994.

PATENTS ISSUED

3,740,607; 3,749,961; 3,893,157; 3,980,919; 4,110,749; 4,207,492; 4,328,466; 5,578,901; 6,800,877; 6,801,002; 7,064,500; 8,459,855; 8,963,895; 9,146,419; 10,620,463; 11,204,516; 11,774,788; 11,841,566.

PUBLICATIONS

Over 100 publications in major technical journals and conference proceedings (Complete listing available on request.)

A monthly column "The Display Continuum" appeared in Information Display Magazine from 1993 to 2003 on various topics of interest to the display community, currently available on-line at “displayconsulting.com”.

Invited seminar presentation at the Society for Information Display Symposium on the "Display Marketplace in the Next Decade."

Multiple presentations of one and two-day courses on current and future display technologies.

Custom Integrated Circuits Conference keynote presentation on "Custom Integrated Circuits: The Challenge of Customer Service in a Changing High-Technology Environment."

REFERENCES

Available on Request.

ARIS SILZARS, PhD -- Expert Witness Work as of December 2024

Past cases that have included depositions and/or trial testimony.

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Washington DC

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District of Delaware

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Investigation No. 337-TA-666
United States International Trade Commission
Washington DC

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Samsung International, Inc. vs. United States of America
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United States Court of International Trade

Eastman Kodak Company vs. AU Optronics Corporation of America, Inc.
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County of Los Angeles

Element Capital Commercial Co. vs. BOE Technology Group Co., LTD
Civil Action No. 2:22-cv-00118 – JRG
United States District Court
Eastern District of Texas – Marshall Division

APPENDIX 2

APPENDIX 2: MATERIALS CONSIDERED

1. U.S. Patent No. 7,233,305 (AUO_0000471)
2. Fle History for U.S. Patent No. 7,233,305 (AUO_0000494; Phenix_AUO_Hisense_0000093)
3. U.S. Patent No. 7,557,788 (AUO_0000483)
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5. Complaint with Exhibits re Case No. 2:23-cv-00477-RWS-RSP
6. Phenix's Disclosure of Asserted Claims and Infringement Contentions with Exhibits
7. AUO's Invalidity Contentions with Exhibits
8. Defendants' PLR 4-2 Proposed Constructions and Identification of Extrinsic Evidence
9. AUO's Extrinsic Evidence re: AUO (AUO_0021912 - AUO_0021944)
10. Phenix's Proposed Constructions (for Phenix/Innolux litigation)
11. Wistron Litigation and IPR Documents (including AUO_0000936-AUO_0002230)Wistron District Court *Markman* Order (AUO_0009658)
12. Innolux IPR Documents (including AUO_0002231-AUO_0003578)
13. Innolux Proposed Constructions
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15. Phenix's PLR 4-2 Proposed Constructions and Identification of Extrinsic Evidence
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17. AUO_0000407-AUO_0000456
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163. PA_00003203 - PA_00003211

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246. PA_00005000 - PA_00005012

247. PA_00005013 - PA_00005025

248. PA_00005026 - PA_00005043

249. PA_00005044 - PA_00005058

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263. PA_00005353 - PA_00005367

APPENDIX 3

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PHENIX LONGHORN LLC,

Plaintiff,

v.

AU OPTRONICS CORPORATION, HISENSE ELECTRONICA MEXICO, S.A. DE C.V., HISENSE USA CORPORATION, HISENSE VISUAL TECHNOLOGY CO., LTD., and DOES 1–10,

Defendants.

CASE NO. 2:23-CV-00477-RWS-RSP

DEFENDANTS' PATENT RULE 4-2 DISCLOSURE OF PRELIMINARY CLAIM CONSTRUCTIONS AND IDENTIFICATION OF EXTRINSIC EVIDENCE

Pursuant to Patent Rule 4-2 and the Court's Docket Control Order (Dkt. 67), Defendant AUO Corporation, Hisense Electronica Mexico, S.A. de C.V., Hisense USA Corporation, and Hisense Visual Technology Co., Ltd., (collectively "Defendants") identify the following preliminary constructions and extrinsic evidence. Defendants make this identification in good faith based on their understanding of Plaintiff Phenix Longhorn LLC's ("Plaintiff") positions and arguments and reserve the right to identify additional or responsive terms or constructions, subtract from, or otherwise amend this list as the parties engage in the claim construction process and related discovery. Defendants incorporate by reference the extrinsic evidence identified in Innolux Corporation's Patent Rule 4-2 disclosures. Defendants reserve the right to rely on any extrinsic evidence identified by Plaintiff.

Claim Term	Preliminary Proposed Claim Construction	Preliminary Identification of Extrinsic Evidence
An integrated circuit for producing voltage signals on a plurality of outputs comprising '305 patent, claim 1	Preamble is a limitation reciting one integrated circuit	Prior art identified in Defendants' preliminary and first amended invalidity contentions. Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.
non-volatile storage cells '305 patent, claims 1, 2	Analog memory cells which retain stored data even when power is removed	Prior art identified in Defendants' preliminary and first amended invalidity contentions. IEEE 100 The Authoritative Dictionary of IEEE Standard Terms (7th Edition, 2000).

		McGraw-Hill Dictionary of Scientific and Technical Terms (5th Edition, 1994). Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.
circuits for programming '305 patent, claim 1	Plain and ordinary meaning	Prior art identified in Defendants' preliminary and first amended invalidity contentions. Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.
coupled to '305 patent, claim 1	Indirectly or directly linked or joined	Prior art identified in Defendants' preliminary and first amended invalidity contentions. Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.

multiplexer for addressing and programming said storage cells '305 patent, claim 1	One or more circuits, excluding an I2C serial bus that couple (1) one input (or one set of inputs) to one of many outputs (or one set of many sets of outputs) or (2) one of many inputs (or one set of many sets of inputs) to one output (or one set of outputs)	Prior art identified in Defendants' preliminary and first amended invalidity contentions. IEEE 100 The Authoritative Dictionary of IEEE Standard Terms (7th Edition, 2000). McGraw-Hill Dictionary of Scientific and Technical Terms (5th Edition, 1994). Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.
programming said storage cells '305 patent, claim 1	Writing data to a storage cell	Prior art identified in Defendants' preliminary and first amended invalidity contentions. Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.
drivers '305 patent, claim 1	Buffers or amplifiers	Prior art identified in Defendants' preliminary and first amended invalidity contentions. IEEE 100 The Authoritative Dictionary of IEEE Standard Terms (7th Edition, 2000). Chambers Science and

		Technology Dictionary (1984). Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.
connected to '305 patent, claim 1	Directly and/or physically linked or joined	Prior art identified in Defendants' preliminary and first amended invalidity contentions. IEEE 100 The Authoritative Dictionary of IEEE Standard Terms (7th Edition, 2000). Webster's Ninth New Collegiate Dictionary (1998). Merriam-Webster's Collegiate Dictionary (10th Edition, 2000). Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.
bank(s) '305 patent, claim 1	Contiguous sections of addressable computer memory arranged in n by m matrix format	Prior art identified in Defendants' preliminary and first amended invalidity contentions. IEEE 100 The Authoritative Dictionary of IEEE Standard Terms (7th Edition, 2000). Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time

		of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.
predetermined gamma reference voltage signal display condition '305 patent, claim 1	A display condition established by the predetermined gamma reference voltage signals based on the application that is being displayed, external environment such as temperature and ambient light, or the personal preference of the user	Prior art identified in Defendants' preliminary and first amended invalidity contentions. IEEE 100 The Authoritative Dictionary of IEEE Standard Terms (7th Edition, 2000). Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.
means to switch between the banks based on one or more external signals '305 patent, claim 1	**Function:** switching between the banks based on one or more external signals; **Structure:** '305 patent at 5:50-6:21; Fig. 4A (B0-B2); Fig. 4B (pins 20, 22, 23); Fig. 5 (Tdamp); Fig. 6 (Bank Select, B0, B1, B2). Wistron CC at 46.	Prior art identified in Defendants' preliminary and first amended invalidity contentions. McGraw-Hill Dictionary of Scientific and Technical Terms (5th Edition, 1994). Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.

external source for the high voltage programming means '305 patent, claim 5	**Function:** programming the non-volatile storage cells using a high voltage signal; **Structure:** (1) (a) a Program Interface, (b) a Vpp input that is used to select the programming mode, (c) the Vpp input also providing the high voltage pulses used during programming of an individual cell, and (d) address inputs A0 and A1 / bank inputs B0, B1, B2 used to select the location being programmed; as described at '305 Patent 6:22-26, Figs. 4A, 4B, 5, or 6 **and/or** (2) (a) a Program Interface, (b) a Vpp input, address inputs A0 and A1, and bank inputs B0, B1, B2 that are used to select the programming mode, (c) the Vpp input also providing the high voltage pulses used during programming of an the [sic] individual cell, and (d) address inputs A0 and A1 and bank inputs B0, B1, B2 used to select the location being programmed; as described at '305 Patent 6:37-53, Figs. 4A, 4B, 5, and 6	Prior art identified in Defendants' preliminary and first amended invalidity contentions. Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '305 patent.
A method of calibrating a liquid crystal display to a desired gamma curve to compensate for panel to panel manufacturing variations comprising the steps '788 patent, claim 1	Preamble is a limitation reciting a calibration method to compensate for panel to panel manufacturing variations	Prior art identified in Defendants' preliminary and first amended invalidity contentions. Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and

		extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '788 patent.
gamma reference control capability '788 patent, claim 1	If the term is not a means plus function term, it is indefinite under 35 U.S.C. § 112. If the term is a means plus function term, it is indefinite for failure to clearly define the claimed function and for lack of a corresponding structure or algorithm in the specification.	Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '788 patent.
control circuit '788 patent, claim 1	If the term is not a means plus function term, it is indefinite under 35 U.S.C. § 112. If the term is a means plus function term, it is indefinite for failure to clearly define the claimed function and for lack of a corresponding structure or algorithm in the specification.	Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '788 patent.
means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor / means for executing said predetermined algorithm '788 patent, claim 1	If the term is not a means plus function term, it is indefinite under 35 U.S.C. § 112. If the term is a means plus function term, it is indefinite for failure to clearly define the claimed function and for lack of a corresponding structure or algorithm in the specification.	Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '788 patent.
predetermined algorithm '788 patent, claim 1	Indefinite under 35 U.S.C. § 112.	Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of

		the patent claims of the '788 patent.
gamma reference voltage levels '788 patent, claim 1	An analog voltage(s) stored in an analog storage cell	Prior art identified in Defendants' preliminary and first amended invalidity contentions. IEEE 100 The Authoritative Dictionary of IEEE Standard Terms (7th Edition, 2000). Aris Silzars may provide testimony regarding how one of ordinary skill in the art at the time of the invention, having reviewed the relevant intrinsic and extrinsic evidence, would have understood the meaning and scope of the term in the context of the patent claims of the '788 patent.

Dated: April 17, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that on April 17, 2025, a true and correct copy of the above document was served on counsel of record via electronic mail.

/s/ *R. Tyler Kendrick*
R. Tyler Kendrick

APPENDIX 4

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PHENIX LONGHORN LLC, Plaintiff, v. AU OPTRONICS CORPORATION, HISENSE ELECTRONICA MEXICO, S.A. DE C.V., HISENSE USA CORPORATION, HISENSE VISUAL TECHNOLOGY CO., LTD., and DOES 1–10, Defendants.	**CIVIL ACTION NO. 2:23-cv-00477-RWS-RSP** **JURY TRIAL DEMANDED**

PLAINTIFF PHENIX LONGHORN LLC'S PRELIMINARY CLAIM CONSTRUCTIONS AND IDENTIFICATION OF EXTRINSIC EVIDENCE

Pursuant to Local Patent Rule 4-2, Plaintiff Phenix Longhorn, LLC ("Plaintiff" or "Phenix") hereby submits its preliminary claim constructions and identification of extrinsic evidence concerning the asserted claims of U.S. Patent No. 7,233,305 (the "'305 Patent") and U.S. Patent No. 7,557,788 (the "'788 Patent") to Defendants AUO Corporation ("AUO"), Hisense Electronica Mexico, S.A. de C.V. ("Hisense Mexico"), Hisense USA Corporation ("Hisense USA"), and Hisense Visual Technology Co., LTD ("Hisense Visual") (collectively, "Defendants"). The following claim constructions are preliminary, and Phenix reserves the right to modify, add to, or otherwise revise these constructions based upon, without limitation, the claim constructions provided by Defendants pursuant to this Local Patent Rule, meet and confer sessions pursuant to the Local Patent Rules, as well as information learned through the course of discovery.

Extrinsic evidence supporting constructions of certain terms is identified below with respect to such terms. Phenix reserves the right to modify, add to, or otherwise revise the identified

extrinsic evidence based upon, without limitation, the claim constructions provided by Defendants pursuant to this Local Patent Rule, meet and confer sessions pursuant to the Local Patent Rules, as well as information learned through the course of discovery. Intrinsic evidence supporting these constructions will be provided in the Joint Claim Construction and Prehearing Statement pursuant to Local Patent Rule 4-3 as well as in the Claim Construction Briefing filed pursuant to Local Patent Rule 4-5.

	'305 Patent		
#	**Term, Phrase, or Clause**	**Asserted Claim(s)**	**Preliminary Construction and Identification of Extrinsic Evidence**
1	"multiplexer"	1	*Preliminary Construction:* • one or more circuits that selectively couple (1) one input (or one set of inputs) to one of many outputs (or one set of many sets of outputs) or (2) one of many inputs (or one set of many sets of inputs) to one output (or one set of outputs) *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
2	"multiplexer for addressing and programming said storage cells"	1	*Preliminary Construction:* • No construction necessary; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)

	'305 Patent		
#	**Term, Phrase, or Clause**	**Asserted Claim(s)**	**Preliminary Construction and Identification of Extrinsic Evidence**
3	"An integrated circuit for producing voltage signals on a plurality of outputs comprising"	1	*Preliminary Construction:* • The preamble of claim 1 is a limitation reciting one integrated circuit. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
4	"coupled to"	1	*Preliminary Construction:* • No construction necessary; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
5	"non-volatile storage cells"	1 and 2	*Preliminary Construction:* • "memory cells which retain stored data even when power is removed" *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
6	"circuits for programming"	1 and 5	*Preliminary Construction:* • No construction necessary; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)

	'305 Patent		
#	**Term, Phrase, or Clause**	**Asserted Claim(s)**	**Preliminary Construction and Identification of Extrinsic Evidence**
7	"programming said storage cells"	1	*Preliminary Construction:* • "writing data to a storage cell" *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
8	"drivers"	1	*Preliminary Construction:* • "buffers or amplifiers" *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
9	"connected to"	1	*Preliminary Construction:* • No construction necessary; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
10	"bank(s)"	1	*Preliminary Construction:* • No construction necessary; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)

	'305 Patent		
#	**Term, Phrase, or Clause**	**Asserted Claim(s)**	**Preliminary Construction and Identification of Extrinsic Evidence**
11	"predetermined gamma reference voltage signal display condition"	1	*Preliminary Construction:* • "a display condition established by the predetermined gamma reference voltage signals based on the application that is being displayed, external environment such as temperature and ambient light, or the personal preference of the user No construction necessary; plain and ordinary meaning" *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
12	"means to switch between the banks based on one or more external signals"	1	*Preliminary Construction:* • Function: switching between the banks based on one or more external signals. • Structure: '305 Patent, 5:50-6:21; Figure. 4A (B0 B2); Figure. 4B (pins 20, 22, 23); Figure. 5 (Tdamp); Figure. 6 (Bank Select, B0, B1, B2). *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)

	'305 Patent		
#	**Term, Phrase, or Clause**	**Asserted Claim(s)**	**Preliminary Construction and Identification of Extrinsic Evidence**
13	"high voltage programming means"	5	*Preliminary Construction:* • Function: programming the non-volatile storage cells using a high voltage signal. • Structure: (1) (a) a Program Interface, (b) a Vpp input that is used to select the programming mode, (c) the Vpp input also providing the high voltage pulses used during programming of an individual cell, and (d) address inputs A0 and A1 / bank inputs B0, B1, B2 used to select the location being programmed; as described at '305 Patent 6:22-36, Figure 4A, Figure 4B, Figure 5 and Figure 6. and/or (2) (a) a Program interface, (b) a Vpp input, address inputs A0 and A1, and bank inputs B0, B1, B2 that are used to select the programming mode, (c) the Vpp input also providing the high voltage pulses used during programming of an the individual cell, and (d) address inputs A0 and A1 and bank inputs B0, B1, B2 used to select the location being programmed; as described at '305 Patent 6:37-53, Figure 4A, Figure 4B, Figure 5 and Figure *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
14	"external source for the high voltage programming means"	5	*Preliminary Construction:* • No construction necessary; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)

	'788 Patent		
#	**Term, Phrase, or Clause**	**Asserted Claim(s)**	**Preliminary Construction and Identification of Extrinsic Evidence**
15	"A method of calibrating a liquid crystal display to a desired gamma curve to compensate for panel to panel manufacturing variations comprising the steps"	1	*Preliminary Construction:* Preamble is limiting; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
16	"predetermined algorithm"	1	*Preliminary Construction:* • No construction necessary; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
17	"gamma reference voltage levels"	1	*Preliminary Construction:* • No construction necessary; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
18	"gamma reference control capability"	1	*Preliminary Construction:* • No construction necessary; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)

	’788 Patent		
#	**Term, Phrase, or Clause**	**Asserted Claim(s)**	**Preliminary Construction and Identification of Extrinsic Evidence**
19	“control circuit”	1	*Preliminary Construction:* • No construction necessary; plain and ordinary meaning. *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)
20	“means for executing a predetermined algorithm”	1	*Preliminary Construction:* • Function: executing a predetermined algorithm. • Structure: programming interface *Preliminary Identification of Extrinsic Evidence*: • Testimony of expert witnesses, including but not limited to Jospeh McAlexander (*See* Attachment A) • *Phenix Longhorn, LLC v. Wistron Corp.*, Case No. 2:17-cv-00711, Dkt. 247, (E.D. Tex Jun. 21, 2019)

Date: April 17, 2025

Respectfully submitted,

By: /s/ Fabio E. Marino

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CERTIFICATE OF SERVICE

I hereby certify that true and correct copies of the foregoing were served on April 17, 2025, on all counsel of record via electronic mail.

By: /s/ *Fabio E. Marino*

Attachment A – Summary of Expected Expert Testimony to be Offered by Plaintiff Phenix Longhorn, LLC Regarding Claim Construction

Joseph McAlexander.

Mr. McAlexander intends to present expert testimony regarding the understanding of a person of ordinary skill in the art of the '305 and '788 Patents, at the time of the invention, with respect to the meaning of certain claim terms and limitations within the Asserted Claims in light of the intrinsic evidence (claims, specification, and prosecution history) and extrinsic evidence. Mr. McAlexander reserves the right to respond to any proposed construction(s) or alleged indefiniteness position advanced by Defendants and their experts.